TECHNICAL MANUAL

SigmaPlus™ Transmitter Series

Exciter Assembly

System M

988-8603-001

T.M. No. 888-8603-001

25-07-01

HARRIS CORPORATION Broadcast Division
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Amendment List Number:	1	**Amendment Date:**	25-07-01
Technical Manual Number:	988-8603 -001	**Technical Manual Name:** SigmaPlus™ Transmitter Series Exciter Assembly System M	
Drawing Set Number:	Not Applicable	**Drawing Set Name:**	Not Applicable
Reason for Amendment:	To confirm effects of adustments made.		

Amendment Instructions:

TITLE PAGE

1. Replace Title page with new one dated 25-07-01.

SECTION II PARTS LIST

2. Replace Section II with updated Section II dated 25-07-01.

Insert this Amendment List sheet at the front of the manual, directly after the title page.

WARNING

THE CURRENTS AND VOLTAGES IN THIS EQUIPMENT ARE DANGEROUS. PERSONNEL MUST AT ALL TIMES OBSERVE SAFETY WARNINGS, INSTRUCTIONS AND REGULATIONS.

This manual is intended as a general guide for trained and qualified personnel who are aware of the dangers inherent in handling potentially hazardous electrical/electronic circuits. It is not intended to contain a complete statement of all safety precautions which should be observed by personnel in using this or other electronic equipment.

The installation, operation, maintenance and service of this equipment involves risks both to personnel and equipment, and must be performed only by qualified personnel exercising due care. HARRIS CORPORATION shall not be responsible for injury or damage resulting from improper procedures or from the use of improperly trained or inexperienced personnel performing such tasks.

During installation and operation of this equipment, local building codes and fire protection standards must be observed. The following National Fire Protection Association (NFPA) standards are recommended as reference:

- Automatic Fire Detectors, No. 72E
- Installation, Maintenance, and Use of Portable Fire Extinguishers, No. 10
- Halogenated Fire Extinguishing Agent Systems, No. 12A

WARNING

ALWAYS DISCONNECT POWER BEFORE OPENING COVERS, DOORS, ENCLOSURES, GATES, PANELS OR SHIELDS. ALWAYS USE GROUNDING STICKS AND SHORT OUT HIGH VOLTAGE POINTS BEFORE SERVICING. NEVER MAKE INTERNAL ADJUSTMENTS, PERFORM MAINTENANCE OR SERVICE WHEN ALONE OR WHEN FATIGUED.

Do not remove, short-circuit or tamper with interlock switches on access covers, doors, enclosures, gates, panels or shields. Keep away from live circuits, know your equipment and don't take chances.

WARNING

IN CASE OF EMERGENCY ENSURE THAT POWER HAS BEEN DISCONNECTED.

WARNING

IF OIL FILLED OR ELECTROLYTIC CAPACITORS ARE UTILIZED IN YOUR EQUIPMENT, AND IF A LEAK OR BULGE IS APPARENT ON THE CAPACITOR CASE WHEN THE UNIT IS OPENED FOR SERVICE OR MAINTENANCE, ALLOW THE UNIT TO COOL DOWN BEFORE ATTEMPTING TO REMOVE THE DEFECTIVE CAPACITOR. DO NOT ATTEMPT TO SERVICE A DEFECTIVE CAPACITOR WHILE IT IS HOT DUE TO THE POSSIBILITY OF A CASE RUPTURE AND SUBSEQUENT INJURY.

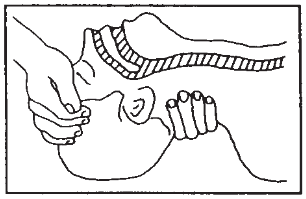
TREATMENT OF ELECTRICAL SHOCK

1. IF VICTIM IS NOT RESPONSIVE FOLLOW THE A-B-CS OF BASIC LIFE SUPPORT.

PLACE VICTIM FLAT ON HIS BACK ON A HARD SURFACE

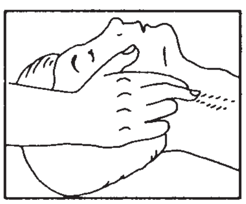
(A) AIRWAY

IF UNCONSCIOUS,
OPEN AIRWAY



LIFT UP NECK
PUSH FOREHEAD BACK
CLEAR OUT MOUTH IF NECESSARY
OBSERVE FOR BREATHING

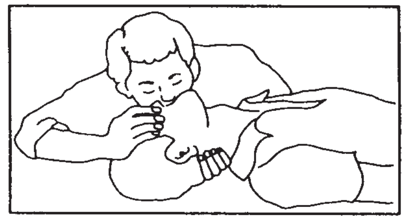
CHECK
CAROTID PULSE



IF PULSE ABSENT,
BEGIN ARTIFICIAL
CIRCULATION

(B) BREATHING

IF NOT BREATHING,
BEGIN ARTIFICIAL BREATHING



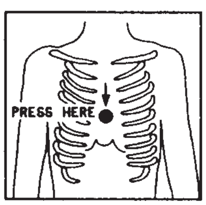
TILT HEAD
PINCH NOSTRILS
MAKE AIRTIGHT SEAL

4 QUICK FULL BREATHS

REMEMBER MOUTH TO MOUTH
RESUSCITATION MUST BE
COMMENCED AS SOON AS POSSIBLE

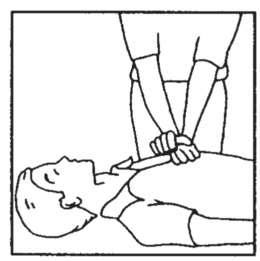
(C) CIRCULATION

DEPRESS STERNUM 1 1/2 TO 2 INCHES



APPROX. RATE OF COMPRESSIONS --80 PER MINUTE { ONE RESCUER: 15 COMPRESSIONS, 2 QUICK BREATHS

APPROX. RATE OF COMPRESSIONS --60 PER MINUTE { TWO RESCUERS: 5 COMPRESSIONS, 1 BREATH



NOTE: DO NOT INTERRUPT RHYTHM OF COMPRESSIONS
WHEN SECOND PERSON IS GIVING BREATH

CALL FOR MEDICAL ASSISTANCE AS SOON AS POSSIBLE.

2. IF VICTIM IS RESPONSIVE.

   A. KEEP THEM WARM
   B. KEEP THEM AS QUIET AS POSSIBLE
   C. LOOSEN THEIR CLOTHING
   D. A RECLINING POSITION IS RECOMMENDED

FIRST-AID

Personnel engaged in the installation, operation, maintenance or servicing of this equipment are urged to become familiar with first-aid theory and practices. The following information is not intended to be complete first-aid procedures, it is a brief and is only to be used as a reference. It is the duty of all personnel using the equipment to be prepared to give adequate Emergency First Aid and thereby prevent avoidable loss of life.

Treatment of Electrical Burns

1. Extensive Burned and Broken Skin

a. Cover area with clean sheet or cloth. (Cleanest available cloth article.)

b. Do not break blisters, remove tissue, remove adhered particles of clothing, or apply any salve or ointment.

c. Treat victim for shock as required.

d. Arrange transportation to a hospital as quickly as possible.

e. If arms or legs are affected keep them elevated.

NOTE

If medical help will not be available within an hour and the victim is conscious and not vomiting, give him a weak solution of salt and soda: 1 level teaspoonful of salt and 1/2 level teaspoonful of baking soda to each quart of water (neither hot or cold). Allow victim to sip slowly about 4 ounces (a half of glass) over a period of 15 minutes. Discontinue fluid if vomiting occurs. (Do not give alcohol.)

2. Less Severe Burns - (1st and 2nd degree)

a. Apply cool (not ice cold) compresses using the cleanest available cloth article.

b. Do not break blisters, remove tissue, remove adhered particles of clothing, or apply salve or ointment.

c. Apply clean dry dressing if necessary.

d. Treat victim for shock as required.

e. Arrange transportation to a hospital as quickly as possible.

f. If arms or legs are affected keep them elevated.

REFERENCES:

ILLINOIS HEART ASSOCIATION

AMERICAN RED CROSS STANDARD FIRST AID AND PERSONAL SAFETY MANUAL (SECOND EDITION)

Refer to the following page for UK First Aid references.

In the United Kingdom, reference should be made to the British Red Cross manual : “FIRST AID MANUAL (6TH EDITION)”. This is also known as the “TRIPARTITE MANUAL” and is also available from the British Red Cross, 9 Grosvenor Crescent, London, SW1X 7EJ or any local Red Cross Branch or recommended stationers.

WARNING SYMBOLS USED IN HARRIS BROADCAST PRODUCTS

Warning symbols are used on labels attached to the equipment at various places to draw the attention of a skilled equipment user to possible hazards.

Generally a notice clarifying the hazard will be displayed or there will be a reference to the technical manual where the user should read the warning notices in this introductory safety section and in the appropriate manual section.

This is a general warning sign indicating CAUTION — RISK OF DANGER. Further guidance is given to avoid dangers to personnel or damage to the equipment.

CAUTION — RISK OF ELECTRICAL SHOCK if safe practices are not adopted. For example, live terminals may be exposed should a cover be removed.

CAUTION — RISK OF NON-IONISING RADIATION during operation if the amplifier, the amplifier accessories or the RF feeder have been installed incorrectly, or are not functioning correctly. (See NON-IONISING RADIATION caution on page Safety-5.)

CAUTION — PRESENCE OF TOXIC MATERIAL.This label on an assembly indicates that a component or components within that assembly contain Beryllium Oxide. If such components are mechanically damaged they could present a TOXIC HAZARD. (See BERYLLIA WARNING notice on page Safety-6.)

NON-IONISING RADIATION (RADIO FREQUENCY/MICROWAVE)

Introduction

RF/Microwave generation (frequency range from 30MHz to 30GHz) occurs in Transmitters and RF Amplifiers.

The Hazard

Exposure of the human body to microwave radiation in excess of $10mW/cm^2$ may be unsafe and can result in blindness or other injury.

The Situation

In addition to the RF power normally emitted from the Transmitter via its output coupling to the co-axial feeder system, some power may be emitted from other apertures (RF leaks). Leaks may also occur from the mating connections in feeder runs, or from faulty equipment.

Safe Practices

In normal operation in accordance with the instructions provided in the transmitter equipment service manual, no hazard will exist if the Amplifier and its accessories have been installed correctly and are functioning properly.

Unless connected to an antenna, NEVER OPERATE THE TRANSMITTER WITHOUT AN RF ENERGY ABSORBING LOAD ATTACHED.

Ensure all input and output RF connections, couplings and flanges are correctly installed and are leakproof.

Ensure that all personnel are prevented from looking into open-ended feeder where radiation due to a fault condition or due to stray antenna pick-up may be present.

Any person accidentally exposed to RF radiation must seek immediate medical attention.

BERYLLIA WARNING

Introduction

Some subassemblies, particularly solid state amplifiers or RF loads, employ transistors or load resistors which contain ‘beryllia’ (Beryllium Oxide). Normally the transistors (e.g. TPV 695A, TPV7025) or loads are perfectly safe to handle, but should such a component suffer mechanical damage the following precautions and special procedures are to be followed.

NEVER ATTEMPT TO DISMANTLE LOADS OR COMPONENTS CONTAINING BERYLLIA.

Handling

Undamaged components can be handled without risk, but there is a toxic hazard if beryllia dust from a damaged component is inhaled or implanted in the skin. It is therefore necessary, if a damaged component must be handled, to cover cuts and abrasions with dressings and to wear disposable gloves. If Beryllia does enter the skin via a cut or abrasion, the affected part must be washed immediately and then treated by qualified medical personnel.

Disposal

The disposal procedure is normally laid down by the Operating Authority and must be strictly adhered to. However, in the absence of such instructions the following points will be of assistance.

The disposal procedure is divided into two categories:

Electrically faulty, but not mechanically damaged

The faulty component should be placed in a polythene bag which is to be sealed and placed in a Beryllia scrap box*.

Mechanically damaged components

Using disposable gloves and tweezers, all visible parts are to be placed in a polythene bag which is to be sealed and placed in a Beryllia scrap box*. Still wearing gloves, clean the area with a damp cloth and then place the cloth and gloves into a polythene bag, seal the bag and place it in a beryllia scrap box*.

The hands must be thoroughly washed after handling damaged components.

* Ideally, the beryllia scrap box is a sealed metal container clearly marked with a warning.

INHIBITED ETHYLENE GLYCOL

Introduction

Some transmitter cooling systems and loads, particularly transmitters operated in colder climates, contain Inhibited Ethylene Glycol. This material is a colourless, viscous liquid which is usually coloured at the customer's request. It is hygroscopic, odourless and relatively non-volatile. It lowers the freezing point of water and is soluble in water, alcohol and acetone. Diluted OR Undiluted it is of low toxicity but, if swallowed, has possible systemic effects. These include Vomiting, Headache and Diarrhoea.

Composition

90% Ethylene Glycol, 10% Inhibitors and Water.

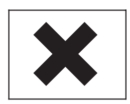
Handling Precautions

Wear safety glasses or safety goggles together with impervious clothing and/or gloves.

Do not eat, drink or smoke whilst using this product. Never transfer to an unlabelled container.

Storage

Store only in hazard labelled containers bearing the symbol



HARMFUL

First Aid

Eyes: Irrigate immediately with copious quantities of water for several minutes. Obtain medical attention if irritation persists.

Skin: Wash immediately with copious quantities of water.

Inhalation: Remove from exposure.

Ingestion: If swallowed, obtain medical attention urgently. Evidence shows that the removal of ethylene glycol from the stomach soon after ingestion may significantly reduce the risk of poisoning. Therefore it is recommended that stomach contents should be emptied under qualified medical supervision as soon as possible following ingestion of this product. Wash out mouth with water.

Disposal Considerations

Disposal must be in accordance with local and national legislation. Unused product may be sent for reclamation and may be incinerated. Used/Contaminated product must be disposed of by an authorised waste contractor to a licensed site. Packaging must be disposed of through an authorised waste contractor.

AIR FILTERS

Introduction

Air cooling of transmitter systems or of parts of systems, necessitates the use of air filters to filter out dust and other extraneous products.

Hazard

Air Filters, after being in use, can contain concentrations of hazardous substances filtered from the surrounding atmosphere.

Servicing

When replacing, cleaning or disposing of the filters, take all necessary precautions.

Exciter Assembly - System M
Table of Contents

Section I
Sigma Plus Exciter Assembly

Section II
Exciter Assembly Overall Description

WARNING: Disconnect primary power prior to servicing

Section III
Parts List

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1.1 General Information

The Sigma Plus Exciter Assembly incorporates all the modules necessary to modulate the required separate visual and aural inputs onto their respective Intermediate Frequency carriers and up-converts the product to the final UHF transmitter frequency. Precorrection is applied to the visual signal before being mixed.

Adjustment of the frequency multiplier and LO/Channel Filters enables the Exciter to cover the entire UHF band from 470MHz to 860MHz.

UHF generation starts when the Master Oscillator provides fundamental drive to the frequency multiplying Harmonic Generator whose UHF output is passed through a Comb Filter before being amplified by a Distribution Amplifier and applied to the UHF Mixer/Up-converter along with the IF signal. The modulated UHF signal is then channel filtered and amplified by the RF Distribution Amplifier to drive the Intermediate Power Amplifier located in the Amplifier cabinet.

The main outputs of the assembly delivers UHF power at a nominal level of 2mW Black (including cable losses) to the Visual RF Corrector, and 2mW CW to the Aural RF Corrector in their respective Amplifier Cubicles.

DC power to the exciter assembly is derived from a Power Supply located on the inside wall of the Contactor and Circuit Breaker drawer.

Depending on power level and tube configuration requirements, the SigmaPlus transmitters include an Exciter/Control Cabinet and/or more Power Amplifier cabinets. When fitted a Control Cabinet will typically contain one or optionally two Exciters, the system control logic, the system control logic, the system controller, transmitter mode controller and, if dual Exciters are fitted, an Exciter Change-over Unit.

Full details of the function, operation and construction of the System Control Panel and Transmitter (Mode) Controller (when fitted) are to be found in SigmaPlus Technical Manual.

1.2 Construction And Layout

In the subsequent description, the modules are referred to by identification letter (as shown on drawings 8928 117 31310/31320 Sh. 1 and 2). Connectors are identified with this letter and connector number e.g. AX1 indicates connector X1 on the Video Processor and Delay assembly. The list of modules and their corresponding identification letter and Part Number are as follows;

- (A) Video Processor and Delay 3913 466 2480001
- (B) Receiver Group Delay 3913 466 2481005
- (C) Differential Phase and I/C Corrector 3913 466 37970
- (D) Vision Modulator and SAW VSB Filter 992 9413 001
- (E) Aural and Visual Corrector 992 9737 021
- (F) Sound Modulator 3913 467 13940
- (G) Group Delay Corrector 3913 466 24830
- (H) Filter Assembly 3913 466 14710(L)/3913 466 14720(U)
- (J) Channel RF Distribution Amplifier 3913 466 78060
- (K) Flywheel Sync Delay 3913 467 12420
- (L) IF Oscillator 4313 466 4032402
- (M) Local Oscillator RF Distribution Amplifier 3913 467 14650
- (N) Filter Assembly 3913 466 14710(L)/3913 466 14720(U)
- (P) Master Oscillator 4313 466 4032403
- (R) Harmonic Generator 3913 467 13220
- (S) Mixer/Up-Converter 3913 467 13260
- (U) Aural Corrector 992 9737 095

The Exciter assembly is constructed using a standard 19 inch equipment rack tray. This is fitted with a locking mechanism located on the drawer runners.

All inputs and outputs are located at the rear of the tray. Additionally, two test points are located inside the front end of the tray.

Forced air cooling is provided by a DC Fan, mounted at the rear of the assembly. Air is drawn in from the front of the exciter tray via holes drilled in the lid, base and front panel. It is then expelled towards, and out from, the rear of the tray.

Note

Module T, Video Delay, is fitted to Exciter B when used in a transmitter system with dedicated Exciters. If this is not the case, Video Processor X4 is linked to Receiver Group Delay X1.

1.3 Functional Description

Refer to the Exciter Block Circuits 8928 117 31310/31320 Sh. 1 and 2.

1.3.1 Video Processing

Baseband Video is fed to the Video Processor Module (A) at AX1 and looped through to other modules, if required, via AX2. If not required this output normally terminates the video line. The module performs the following functions:

a. Suppresses hum and noise on the incoming video.
b. Separates the picture content from the sync pulses and processes each separately. The sync pulses are suppressed and re-generated, the new pulses can be either reinserted or fed out separately.
c. Clamps the black level to 0V.
d. Limits peak white excursions of the luminance signal.
e. Provides output video with peak white at +0.7V.
f. Provides a composite sync pulse output, with blanking level at 0V, and peak sync at +1V.
g. Provides an INHIBIT logic output in the event of unsatisfactory input sync pulses.

h. Provides video mute from external input.

The video content is fed out via connector AX2, and the sync output via AX3 to the Flywheel Sync Delay Generator.

The VIDEO PROCESSOR MUTE signal, generated by the Flywheel Sync Delay Generator, is routed to the Video Processor module AX5 pin 7 to inhibit the video output (AX4). This signal becomes active when a discontinuity is detected in the sync train. This would indicate that there is a possibility of overdriving the Transmitter amplifiers.

SYNC NORMAL is indicated by a green LED.

1.3.2 Flywheel Sync Delay Generator

The Flywheel Sync Delay Generator (K) prevents disturbances in the video signal from overdriving the RF amplifier stages. This is achieved by generating a VIDEO MUTE signal which is supplied to the Video Processor Module.

To ensure that there is no loss of gain-control in the transition between ‘Video On’ and ‘Video Off’, delayed sync pulses are also generated on this board. These pulses are used in the linearity corrector and are also fed to X5 on the rear of the tray.

VIDEO MUTE is indicated by a red LED.

1.3.3 Receiver Group Delay

Pre-correction for the Receiver Group Delay module (B) is applied to the processed video signal to compensate for domestic receiver characteristics. A choice of one of seven predetermined responses is available. The module is passive and has input and output connections on BX1 and BX4 respectively.

1.3.4 Differential Phase and Intercarrier Phase Correction

In the Differential Phase and I/C Corrector Module, differential phase correction is applied to the video signal supplied to the Modulator and SAW VSB Filter (D) via an ‘Elastic Delay Line’ in which the required phase changes are produced by creating a variable delay as a function of picture luminance level. The video signal is output via CX4.

Carrier phase correction is applied to the IF CW signal prior to vision modulation The same video signal is used to drive the Corrector as for differential phase. The IF is output via CX4.

1.3.5 Vision IF Modulation and VSB Filtering

The video signal from the Differential Phase and I/C Corrector (CX3) is connected to the Modulator and SAW VSB Filter Assembly (D) via DX1. The video modulated IF is passed through a SAW filter which contains the necessary VSB characteristics. It is then output at DX4 at a level equivalent to 1mW peak sync. The SAW filter is enclosed in a temperature-controlled oven.

The vision IF input is fed in at DX2. A DSB output is provided for test purposes, selected by an internal changeover link and available at DX7.

IF NORMAL is indicated by a green LED.

1.3.6 Sound Modulator

This module (F) is designed to accept a combination of inputs. These consist of; baseband balanced monophonic (FX10) or stereophonic audio (FX8), Secondary Audio Programming (SAP) and professional channels (FX4 and FX11), in which all the services modulate an FM subcarrier, as described in the BTSC system.

IF enters the module via FX9 and the main output modulated signal to the mixer is routed to FX1. MUTE, SIGNAL PRESENT and LOOP LOCKED indications are displayed via red, green and red LEDs respectively.

1.3.7 IF Oscillator

The IF Oscillator (L) is identical, except in frequency, to the Master Oscillator (P) and contains a third-overtone crystal oscillator housed in a temperature controlled oven. By selection of the required crystal, the oscillator is capable of producing frequencies in the range 37MHz to 66MHz.

Three signal outputs are provided, each set to a nominal 1mW into 50 ohms.

Fine frequency control is achieved by adjustment of the internal potentiometer or by applying an external control voltage.

IF NORMAL on all three outputs is indicated by a green LED.

1.3.8 Group Delay Correction

The Group Delay Corrector Assembly (G), contains six active, all-pass equaliser networks. These circuits provide group delay corrections to compensate for errors introduced mainly by the associated power amplifiers and vision sound combiner. The corrections are adjusted during the setting-up of the transmitter system.

1.3.9 Aural and Visual Corrector Assembly

The Aural and Visual Corrector Assembly (E) is a dual purpose assembly that provides IF pre-correction for aural and visual signals and then combines the resulting signals to give a single, multiplexed output.

Linearity correction is applied to the visual signal, entering via EX1, while phase modulation is applied to the aural signal entering via EX2.

Back-end AGC is used to stabilise the corrected visual and aural outputs independently and uses the delayed sync pulses (EX6, looped through EX7) from the flywheel module to sample the incoming signals.

After pre-correction and AGC has been applied the two signals are combined to the required ratio and amplified to give output at EX9.

The AGC VOLTAGE for both visual and aural loops are monitored on board and displayed as 10-segment moving dot green bar graphs.

1.3.10 Aural Corrector Assembly

This unit accepts separate visual IF (UX11) and aural IF (UX6) inputs and provides a combined IF output (UX1) with aural precorrection. The aural AGC keeps the visual to aural ratio constant regardless of the level of correction or level of temperature changes.

To achieve aural pre-correction the aural signal is combined with a sample of the vision signal and applied simultaneously to two identical non-linear circuits. The outputs of these two non-linear circuits are summed to give the pre-corrected aural signal. Because of the phase relationship between the two non-linear paths, the vision sample signal is cancelled and only the aural signal remains. The resulting signal carries inter-modulation products that are opposite to those generated in the power amplifier.

Sync pulses are fed to the PCB from the Aural and Visual Corrector assembly and are also looped-through the PCB leaving at UX8.

1.3.11 Master Oscillator

The Master Oscillator (P) is identical to the IF Oscillator (L) except for the crystal frequency being selected for correct frequency multiplication to produce the local oscillator UHF frequency. Levels of 1mW CW are set at PX1, PX2, PX3.

1.3.12 Harmonic Generator

The Harmonic Generator (R) produces harmonics of the master oscillator output, from which a local oscillator frequency is derived to produce sound and vision RF outputs. These are fed into the module from the master oscillator at RX1. The spectrum or ‘comb of frequencies are equally spaced at multiples of the exciting frequency and are fed to the output RX2. Tuning of the multiplier is achieved by adjustment of the two matching capacitors in conjunction with the step recovery diode bias potentiometer.

1.3.13 Local Oscillator Comb Filter

The Comb Filter (N) is a four-section passive filter with independent input and output match adjustments; at NX1 and NX2 respectively. It is used to select the required harmonic produced by the frequency multiplier so that it may be applied to the Mixer/Up-converter.

Two filters are available Lower (L) and Upper (U). (L) covers the frequencies in the lower band, 470 to 696MHz and (U) covering frequencies in the upper band, 650 to 930MHz.

1.3.14 Local Oscillator RF Distribution Amplifier

The RF Distribution Amplifier (M) is an expandable module allowing any combination of between two to four UHF outputs.

In this application the Harmonic Generator, at a nominal 1mW peak sync, enters the module via MX1. It passes through a matching pad and amplifier before being attenuated by a variable attenuator controlled via a potentiometer. The potentiometer is accessible through the module lid.

The controlled signal is then amplified by two amplifiers and exits the module via MX2 and MX3.

1.3.15 Mixer/Up-converter

The Mixer/Up-converter Assembly (S) uses one circuit for combined aural and vision signals. The local oscillator signal is fed in from the Distribution Amplifier at SX3 and is mixed with the modulated aural and visual IF signal. This signal is then amplified before being fed via SX2 to the next stage of the mixer assembly at Filter (H). An IF monitor output is provided when required for the purpose of ALC of the mixer input.

1.3.16 Channel Comb Filter

The Channel Comb Filters (H) is identical in construction to that of the local oscillator filter. It is set up in much the same way so as to provide good out-of-band rejection to unwanted mixer products. Input and output is at HX1 and HX2 respectively.

Two filters are available, one (L), covering frequencies in the lower band, 470 to 696MHz, and the other (U), covering frequencies in the upper band, 650 to 930MHz.

1.3.17 Channel RF Distribution Amplifier

The RF Distribution Amplifier (J) used here is similar in operation to that of the Local Oscillator Distribution Amplifier, except that the number of outputs available may differ and the output level is lower.

1.3.18 Monitoring

1.3.18.1 Local Facilities

Basic monitoring facilities for the Sigma Exciter Assembly are provided inside the tray on the front panel. This consists of two BNC coaxial sockets with floating leads terminated in SMB sockets, for connection of module inputs/outputs to external test equipment.

1.3.18.2 Remote Facilities

Provision is made for remote monitoring, via multi-way connector X8.

The monitoring signals available are as follows:

a. Pin 1 - AURAL IF OK
b. Pin 2 - MASTER OSCILLATOR OK
c. Pin 3 - SYSTEM NORMAL
d. Pin 4 - SYSTEM NORMAL
e. Pin 6 - 0V
f. Pin 7 - 38.9 MHz OSCILLATOR OK

1.3.18.3 System Normal Loop

The ‘system normal’ loop external connections are made through connector X8, pins 3 and 4. Internally the loop is completed via the Aural and Visual Corrector - EX5 pin 5 and EX5 pin 6 and the Sound Modulator - FX5 pin 5 and FX5 pin 6.

1.3.19 Power Distribution

Power to the Exciter Assembly is routed via the PSU Distribution PCB (located in the Control Cubicle - see section 1.3.19), to the connector X9 on the rear of the tray. From here it is divided on the internal connectors X18, X19, X20. The supplies for each module are selected in the cableform and are routed to their respective module connectors (X5 in each case). This cableform and connector assembly also forms the monitoring routing for the Exciter.

1.3.20 PSU Distribution PCB

The PSU Distribution PCB (not part of the Exciter assembly) contains connectors, fuses and various LEDs. The PCB accepts power supply outputs from PSU A and PSU B and routes them via the fuses and LEDs to the various assemblies within the drive system. The LEDs indicate when a supply is present. Fuses are rated according to requirement with supplies of 0V, +5V, +12V, -12V and +24V present on the board.

1.4 Exciter Setting-up Procedures

1.4.1 General

The individual modules are assembled in the exciter tray after having been fully tested. Those which perform correction should have the correction turned off on initial installation; therefore no setting up without the parent SigmaPlus amplifier should be necessary (refer to section 1.4.2). However, if a problem occurs, the following guide may be applied in an attempt to rectify the situation:

a. Video Processing: Check that video processor output at AX4 is 1V peak to peak with +0.7V video, -0.3V sync, black level at 0V. The green LED should be illuminated.

b. IF and Master Oscillator Generation: Check that there is 1mW CW at LX1, LX2, LX3, PX1, PX2, PX3 and both green LEDs are illuminated.

c. Differential Phase and I/C Correction: Check that the IF Oscillator input at CX2 is at 1mW CW and the video at CX3 is 1V pk/pk.

d. Vision IF Modulation: Check that the IF input at DX2 is 1mW CW, the modulation depth is correct for the application at 1mW peak sync on DX4 and the green LED is illuminated.

e. Flywheel Sync Delay generation: Check that the LED is extinguished.

f. Sound Modulation: Check that the level at FX1 is 1mW CW and that only the green LED is illuminated.

g. Group Delay Corrector: Check there is a 1mW peak sync visual signal at EX1 and EX4.

h. Harmonic Generator: Check that there is 1mW CW Master Oscillator at RX1 and a comb of frequencies is present at the output, RX2.

i. Local Oscillator: Check that the required Local Oscillator UHF tone is present at LX2 and that the amplified output, MX3, of the RF DA is a nominal 5mW CW.

j. Mixer Stage: Check the following:

1. Visual IF input of 0.5mW peak sync at SX4.
2. Visual LO input of 6mW at SX3.
3. 2mW black at X4 of the RF Corrector on the Visual Amplifier Cabinet front panel.
4. Adjust RF Amplifier output to 2mW black (no sound) level at the input of the Transmitter RF connector (approximately 3mW out of J/X2).

Details of the overall setting up procedure are given in the associated System Manual and a procedure for setting up the corrections is given in section 1.4.2.

1.4.2 Setting Up the Corrections

1.4.2.1 Initial Conditions

This procedure applies to the SigmaPlus Transmitter**,** driven by the Solid State IPA :

a. The IOT is to be tuned flat from Fv 1dB -1.0MHz to Fv +6.5MHz.

b. All IF correction circuits should be either disabled or bypassed for the start of the procedure.

c. Ensure switch S2, Sync Stab, located on the rear of the IF Linearity Corrector, is in the down position.

1.4.2.2 Correction Procedure

a. Set up Feed Forward. Modulate the transmitter with a RAMP. Adjust input cavity for minimum inputs.

b. Adjust the Linearity Corrector whilst observing inputs at Transmitter outputs, for minimum.

c. Apply ICPM correction from the exciter until ICPM is better than 2 .

d. Apply linearity correction at IF using only the wideband correction sections to obtain better than 5% differential gain at sub-carrier frequency and better than 10% low frequency non-linearity.

e. Re-check ICPM and make any necessary minor improvements.

f. Correct Differential Phase to within 3° .

g. Remove staircase video input and connect video input from SBA with 20% sweep on mid-grey pedestal. Observe Amplitude frequency response on the spectrum analyser (10dB/division) and check that the lower sideband is more than 20dB below the wanted sideband.

h. If the above complies, check lower sideband amplitude at white and black pedestals where it should also meet the -20dB requirement.

i. If the lower sideband is out of specification then experiment with linearity correction by adjusting at the Aural and Visual Corrector to determine whether there is another combination of the correction controls that will improve linearity and still produce the required linearity and differential gain. Include in the adjustments the group delay corrector at the output of the Aural and Visual Corrector. The frequency and ‘Q’ of the tuned circuit should be adjusted to give best cancellation of the lower sideband.

Notes:

1. Avoid adjustment of LF linearity corrections, as they will cause a poor result of sideband reinsertion.

2. Large adjustments of Black/Sync stretch will cause ICPM at sync to be over-corrected.

1.4.3 Exciter Assembly, Module Designations

A Video Processor

B Receiver Group Delay

C Differential Phase and I/C Corrector

D Modulator and SAW VSB Filter

E Aural and Visual Corrector

F Sound Modulator

G Group Delay Corrector

H Filter

J Channel RF Distribution Amplifier

K Flywheel Sync Delay

L IF Oscillator

M Master Oscillator

N Comb Line Filter

R Harmonic Generator

S Mixer/Up-converter

T Video Delay

U Aural Corrector

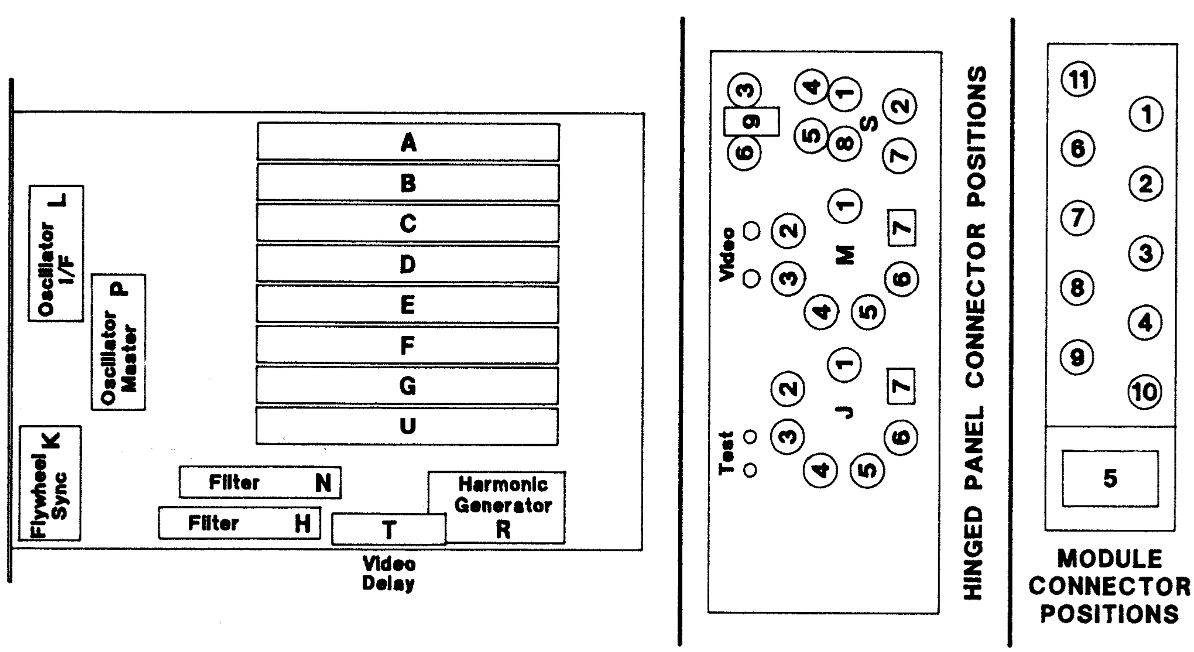

Figure 1-1 Exciter Assembly - Component Layout

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2.1 General Information

The Sigma Plus Exciter Assembly provides UHF drive power for the Intermediate Power Amplifier (IPA). It accepts baseband video and audio inputs, modulating them onto their respective Intermediate Frequency carriers where pre-correction is applied and up-converting the combined visual/aural signal to the final RF UHF transmitter frequency.

Adjustment of the frequency multiplier and LO/Channel Filters enables the Exciter to cover the entire UHF band from 470MHz to 860MHz.

UHF generation starts when the Master Oscillator provides fundamental drive to the frequency multiplying Harmonic Generator whose UHF output is passed through a Comb Filter before being amplified by a Distribution Amplifier and applied to the UHF Mixer along with the IF signal. The modulated UHF signal is the channel filtered and amplified by the RF Distribution Amplifier to drive the Intermediate Power Amplifier located in the Amplifier cabinet.

The main outputs of the assembly delivers UHF power at a nominal level of 2mW black (including cable losses) to Visual RF Corrector, and 2mW CW to the Aural RF Corrector in their respective Amplifier Cubicles.

DC power to the exciter assembly is derived from a Switched Mode Power Supply located on the inside wall of the Control Cubicle.

The Exciter Assembly installation for each transmitter is mounted in the Control Cabinet. Also located in this cabinet are:

a. the System Control Panel
b. the Transmitter (Mode) Controller
c. the Exciter Changeover Unit (if dual Exciters fitted)

The Transmitter Controller controls the complete Transmitter system. Full details of function, operation and construction are given in the SigmaPlus Technical Manual.

2.2 Video Processing Module

2.2.1 General Description

The Video Processing Module is designed to operate in one of two modes:

a. Normal Mode, in which a composite video signal is separated into its video and sync components. These are separately processed and then amalgamated to form the output video signal.
b. Pulser Operation, in which the sync and video signals remain separated.

2.2.2 Normal Operation

The processes performed during normal operation are as follows:

a. Suppression of longitudinal hum and other disturbances present in the video signal including:
   1. Spurious pulses,
   2. Random noise,
   3. Hum from 50Hz to 400Hz,
   4. RF interference from 15kHz to 6MHz,
   5. Frequency response errors.
b. Stabilisation of the amplitude and shape of the new sync pulse.
c. Fixture of black level at 0V (ground),
d. Limitation of peak white excursion,
e. Generation of indications that input and output sync levels are within specified limits.

The operation of the unit in the normal mode is summarised in the functional block diagram in 3913 466 24801 Sh. 136-1.

2.2.3 Pulser Operation

In the pulser operation mode the module performs the following functions:

a. Suppression of longitudinal hum and other disturbances present in the video signal including :
   1. Spurious pulses,
   2. Random noise,
   3. Hum from 50Hz to 400Hz,
   4. RF interference from 15kHz to 6MHz,
   5. Frequency response errors.
b. Provision of a sync output for external application.
c. Fixture of black level at 0V (ground),
d. Limitation of peak white excursion.

2.2.4 Construction

The unit is built on to a printed wiring board fitted into a module frame which is enclosed in a metal case. Access to controls for adjustments is obtained through holes in the case. All connections are by plug and socket.

A light-emitting diode on the front panel of the module casing indicates normal input and output syncs when illuminated, for normal operation, and normal input syncs in the pulser mode.

2.2.5 Technical Data

a. Input Impedance :
   75 ohms.
b. Return Loss :
   40dB up to 6MHz.
c. Input Level :
   1V pk-pk nominal, with a DC level of ±5V.
d. Video Input Gain Control :
   ±3dB
e. Output Impedance :
   75 ohms
f. Output Levels :

1. Normal Operation :
   a) Reinserted sync :
      300mV pk-pk adjustable
   b) Picture :
      700mV pk-pk, adjustable.
   c) Blanking Level :
      0V (ground). In the absence of video the output remains at 0V.
   d) Reinserted Sync Pulse Rise and Fall Times :
      Leading and trailing edges independently adjustable. Stable for input sync variations of +3 to -6dB. See details on Figure 2-13.
   e) Sync Pulse Amplitude Stabilisation :
      Output sync constant within ±8mV for input variations of +3 to -6dB.
   f) Sync Pulse Timings :
      ±50ns of leading and trailing edges at half amplitude points with respect to trailing edge of picture.
2. Pulser Operation :
   a) Composite Sync Pulse :
      Sync tip +1V ±0.2V. Blanking level 0V
   b) Video :
      Blanking level 0V Peak white +0.7V
3. Longitudinal Currents in the Input Cable (Common Mode Rejection) :
   Better than 26dB rejection for frequencies of 50Hz to 300Hz
4. Clamp Performance:
   a) Low-frequency Loss On Input :
      No failure of normal operation when a 16µF capacitor is connected in series with 75 ohm source and load impedances, with a 50Hz composite square wave applied to the input, for sync amplitude +3 -6dB.
   b) Very low frequency Response :
      Transient crushing of staircase waveform or sync 2%. (5-step staircase once every 4th line - intervening lines varied from black to white at 0.3Hz or less.)
   c) RF Interference :
      No failure of normal operation in the presence of interfering signals of:
      0-1MHz at 50mV
      1-3MHz at 150mV
      3-6MHz at 300mV
      for an input signal range of+3dB to -6dB with spurious pulses as defined below but reduced in amplitude in the same proportion as sync.
5. Hum Rejection (Differential Mode) :
   Better than 26dB, with 500mV pk-pk of 50Hz sine wave added to input.
6. Noise Conversion, HF to LF, Defined as Output Signal to Noise Ratio minus Input Signal to Noise Ratio :
   Better than 16dB for 40dB input S/N ratio and 22dB for 24dB input S/N ratio, for hum rejection of 26dB. 6dB further improvement is possible if hum rejection is lowered to 20dB (AOT R28 in the main clamp determines “hardness”).
   Input noise filtered to remove components above 5.5MHz and below 15kHz.
   Output S/N ratio measured in the range 40Hz to 7.5kHz.
7. Spurious Pulses on the Input (Small) :
   No failure of normal operation when pulses of up to 1.5µs duration extending to 0.6V below black level are added to input once per field.
8. Spurious Pulses on the Input (Large) :
   No more than one incorrectly timed clamp pulse and no more than two clamp pulses missing when pulses of 1.5µs to 64µs 0.6V below black level are added once per field.
9. Clamp Disturbances :
   a) Synchronous (Locked) Disturbances :
      1% peak.
   b) Asynchronous (Moving) Disturbances :
      Better than - 50dB un-weighted noise w.r.t. peak white picture amplitude.
10. Differential Gain :
    1% with 500mV of hum added to input and all combinations of staircase and bounce waveforms.
11. Differential Phase :
    1° with 500mV of hum added to input and for all combinations of staircase and bounce waveforms.
12. Linearity :
    1% non-linearity with 500mV of hum added to input and for all combinations of staircase and bounce waveforms.
13. Phase Error :
    Less than 1° with input and output burst vectors superimposed and error measured on colour vectors.

2.2.6 Technical Description

Refer to the functional block diagram, 3913 466 24800 Sh. 136-1 and the circuit diagram, Sh. 130-1.

2.2.6.1 Video Signal Path

2.2.6.1.1 *Input Amplifier*

This stage performs the following functions:

a. Suppresses longitudinal hum and other common-mode interference, such as RF. This function is performed by the differential amplifier V1, a dual FET.
b. Raises the input video to 6V pk-pk to drive the delay line.
c. Drives the side chain low-pass filter R24, R116, R117, C44, C45, V45 with 3V pk-pk video.

Composite video entering the unit at X1 at a level of 1V p-p is applied to the non-inverting input of V1, which has differential inputs. At the same time it is looped through to X2 where it is terminated in 75 ohms. If required, instead of being terminated, it can be looped through to another module accepting video. The screens of X1 and X2 are kept floating above earth by R2 and are connected to the inverting input of V1. Common-mode signals such as longitudinal hum on the incoming video are developed across R2 and thus applied to both differential inputs so that they are cancelled out. V1 has a high input impedance, so that there is negligible shunting of the 75 ohm module's input impedance, and a high return loss is produced enabling the video to be looped through at high impedance.

The gain is stabilised by a feedback loop R14, R9, R15, C6. Another feedback loop R19, A1, R21, R13 keeps the output black level at near 0V by controlling the voltage at V1A gate, the non-inverting input; the loop time constant is set at 1 second by C1, R13. This loop also ensures that with no video input the quiescent output voltage from V9 is 0V. Gain can be varied by means of R9 to cater for differences in input amplitude and is adjusted to obtain 6V pk-pk amplitude.

2.2.6.2 Delay Line

The purpose of the delay line is to delay the incoming video so that blanking and re-inserted sync have the correct time relationship to it. These would otherwise arrive late because of delays introduced by the sync separator and the low-pass filter.

The precise relationship may be adjusted by tuning the side chain LP filter by means of C45 while observing the relationship between picture timing and re-constituted sync. The output of the delay line is 3V pk-pk.

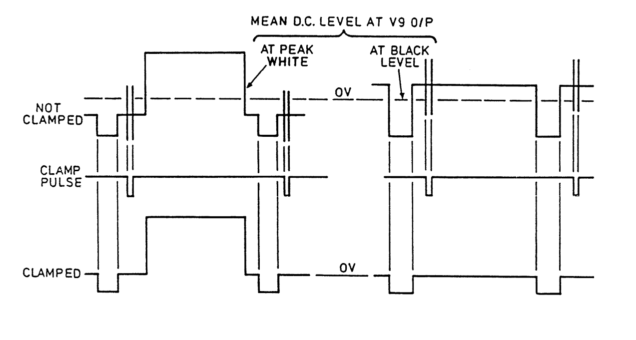


Figure 2-1 Clamping pulses

2.2.6.3 Clamping Operation

The main clamp (V13, V14) is basically a switch operated by a logic signal from the main clamp generator A10B. The signal at V9 emitter has an arbitrary mean DC level because of AC coupling through C1 at the video input. The DC level in the blanking period is clamped at 0V, as shown in Figure 2-1 **,** to avoid variations in modulation depth and black level power at the visual modulator output.

Main clamp pulses of 3µs duration from the clamp generator close switch V14 which short-circuits V16 input to ground (0V) during the back porch. When the colour burst is present in the back porch, disturbances to both black level and the burst itself could occur; to black level because of phase alternation, and to the colour burst because it is effectively short-circuited by the clamp. This is overcome by including the burst trap L4, C14, R29 in the clamp path; it is tuned for minimum phase error using a Vectorscope. R29 damps the tuned circuit and so prevents it ringing when the clamp pulse ceases.

2.2.6.4 Sync Amplitude Stabilisation

Amplitude stabilisation of the sync pulses is performed in three stages as follows:

- Elimination of the sync pulse at the output of the unity-gain balanced amplifier V16 (see 2.2.6.5)
- Production of a new sync pulse (see 2.2.7.9).
- Re-insertion of the new sync pulse into the video signal in V17/V18 (see 2.2.6.6).

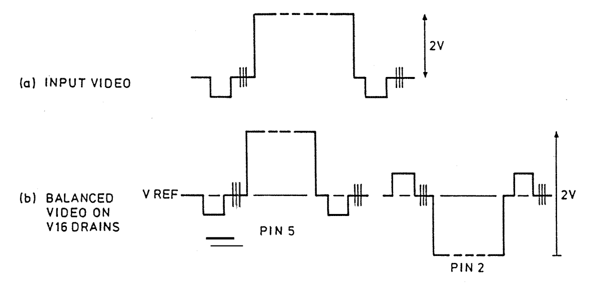


Figure 2-2 Sync pulse suppression

2.2.6.5 Sync Pulse Suppression

The signal at V16 outputs, i.e. across V15, is at high impedance (approximately 2k ohms) and has a well defined black level voltage.

Figure 2-2 (b) illustrates how the balanced video would appear if blanking were disabled.

After the video signal is clamped, so that black level is fixed at 0V, the existing sync pulses are suppressed, as follows (refer to the functional schematic).

Blanking is performed by the low-capacitance switch V15, which when fed with sync blanking pulses from A2C short-circuits the balanced outputs of V16 together, thus eliminating the sync pulses.

Any spikes produced by this action are reduced by feeding some of the switching pulse edges to V16B input via C16, along with some DC bias from the potential divider R38, R41, R42 to reduce offset effects.

2.2.6.6 Balance/Unbalanced Conversion and Sync Pulse Re-insertion

Balanced non-composite video is now fed to the balance-to-unbalance converter V17-V19. New sync generated in the sync shaping circuit V46-V54 (see 2.2.7.9) is added in this stage. The output of the balance-to-unbalance converter stage is 3V pk-pk.

Then,

Gain of the inverting input (V18) :

$$A1 = \frac{R51}{R43} = 1$$

Note: R51 = R43 trimmed by R130.

Gain of the non-inverting input (V17):

$$\underline{\underline{A2}} = \left(1 + \frac{Rx}{Ry}\right)\left(\frac{Rx}{Rx + Ry}\right)$$

$$= \left(1 + \frac{4.7}{4.7}\right)\left(\frac{4.7}{9.4}\right) = \underline{\underline{1}}$$

The blanking level, see Figure 2-3, offset voltages (approximately +10V) cancel out in the common mode, leaving black level at 0V again.

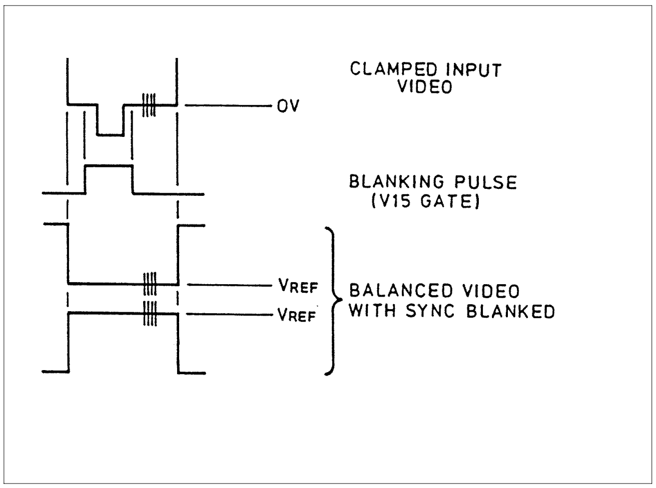


Figure 2-3 Blanking

2.2.6.7 Peak White Limiter

Peak white excursions (beyond a pre-determined level) are suppressed as follows.

When peak white exceeds the reference voltage V_R set by R60 (PEAK WHITE LIMITER) at V22 base, V21 base-emitter junction becomes reverse-biased and the emitter current through R56 switches from V21 (video signal) to V22 (peak white limiting). The output is then $V_R + V_{be}$.

For voltages below the reference, V21 behaves as an emitter follower. V20 and V23 are complimentary emitter followers, eliminating V_{be} offset and thermal drift.

In order that the limiter should not effect chrominance information, this is fed forward through a series tuned circuit L5, C23 to V23 and then superimposed on the reference voltage. As it is a low-Q circuit, frequencies above approximately 1MHz are also fed through; hence the limiter has little effect on frequencies above 1MHz.

2.2.6.8 Bar Tilt Compensation and HF Boost

A Bar Tilt Compensator and HF Boost printed circuit board is included in the output of the peak white limiter to produce a high-frequency video lift, where L1 adjusts the fre-

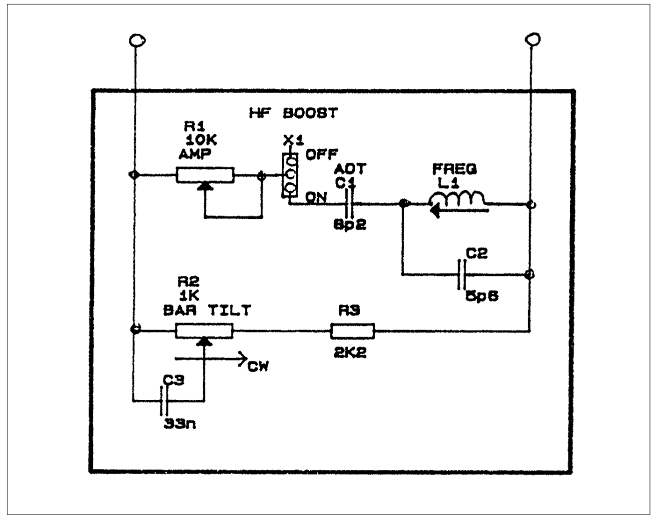


Figure 2-4 Bar Tilt and HF Boost circuit

quency and R1 the extent of the lift. R2 is adjusted to give the required Bar Tilt on final Transmitter setting up.

The board can be used to obtain both HF Boost and Bar Tilt compensation together. If HF Boost only is required, Bar Tilt can be turned OFF by turning R2 fully anti-clockwise. If Bar Tilt only is required, HF Boost can be turned off by moving link X1 to the OFF position. Figure 2-4 details the circuit.

.

Notes

(1) When this PCB is used with the Video Processor, R52 on the main PCB must be removed and the boost PCB is then a permanent Fixture.
(2) To turn OFF Bar Tilt compensation, turn R2 Fully counter-clockwise.
(3) To turn OFF HF Boost, move link X1 to the OFF position .
(4) C1 is an Adjust On Test component for best boost compensation.

2.2.6.9 Output Amplifier

V24-V27 form an operational amplifier of unity gain feeding the 75 ohm video outlet at X4. Video is applied to the non-inverting input at V24 base. The output stage current is set by R70 whose value is selected on test for a current of 50mA.

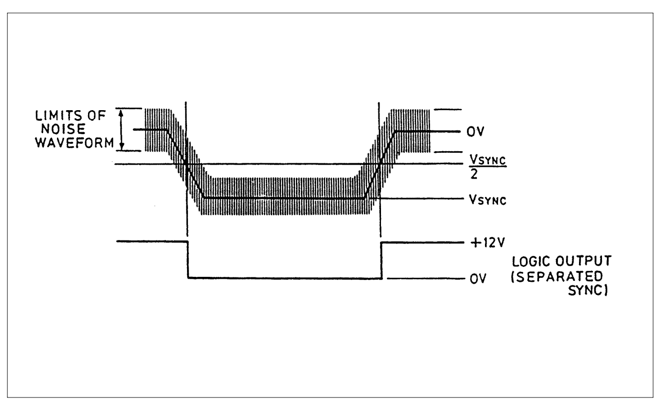


Figure 2-5 Sync separation

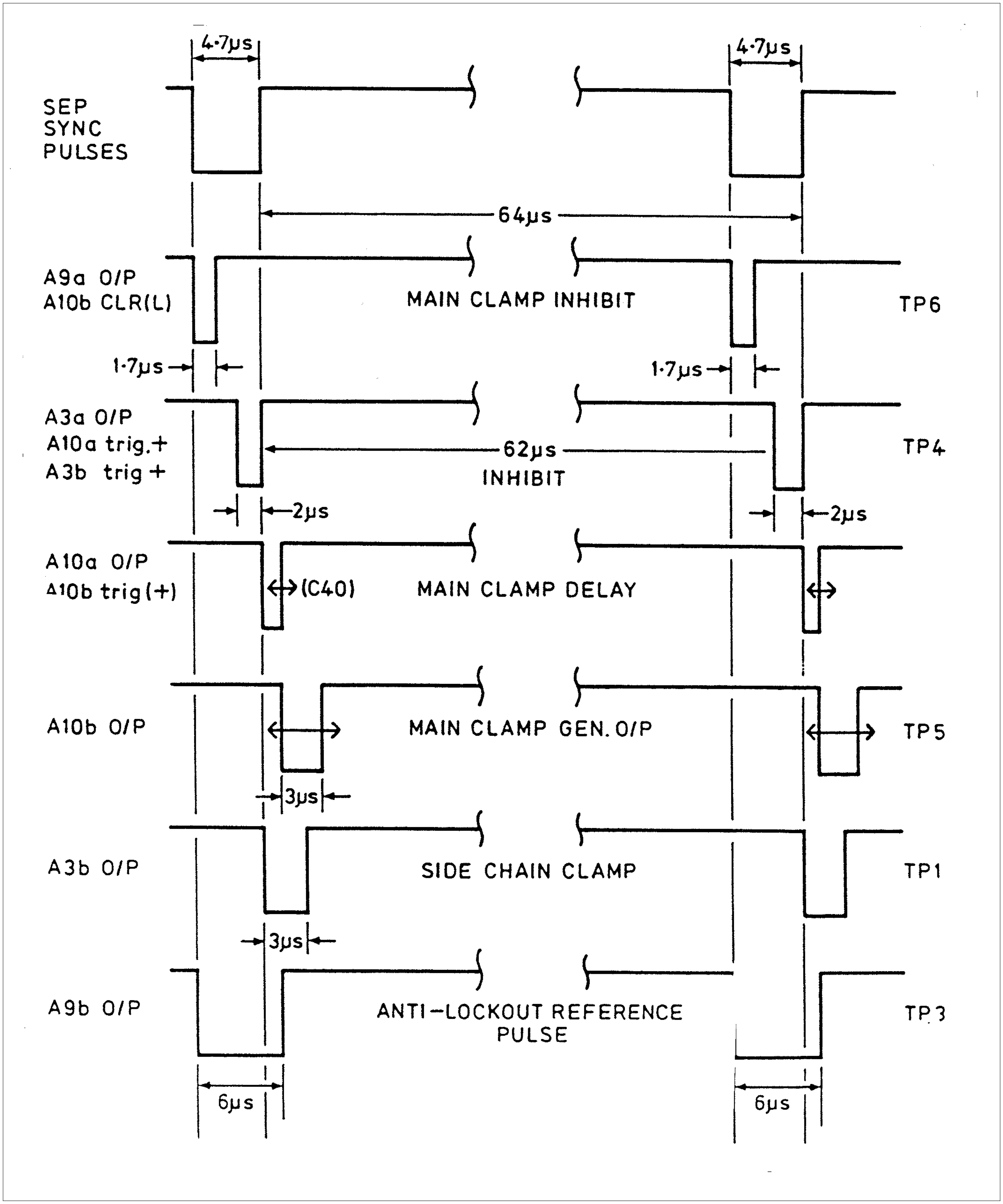


Figure 2-6 Sync pulse waveforms

In normal operation R62 and R63 form an L-section attenuator to reduce the video output amplitude, before the 75 ohm resistor, to 2V pk-pk.

During pulser operation the video output from X4 is a syncless signal, with blanking level at 0V and peak white at 0.7V.

2.2.7 Side Chain

The side chain includes circuits for the following functions:

a. Input video LP filter.
b. Sync separation.
c. Sync blanking pulse generation.
d. Monostables for pulse timing and generation.

e. Main clamp generation.
f. Side clamp generation.
g. Anti-lockout.
h. New sync shaper.
i. Pulser outputs.
j. Input sync high/low measurement

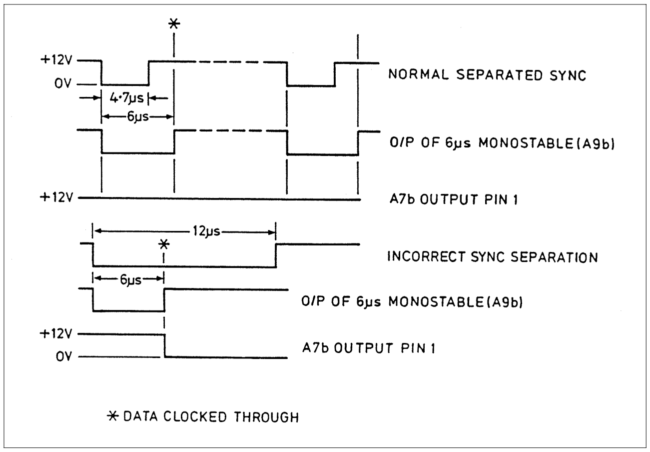


Figure 2-7 Anti-lockout circuit (a)

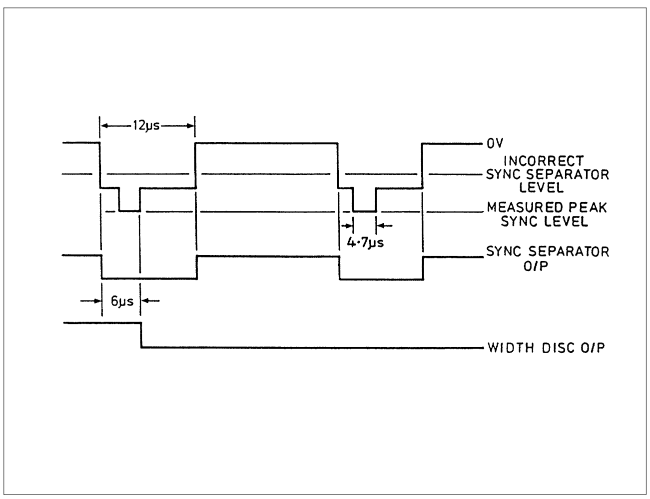


Figure 2-8 Anti-lockout circuit (b)

2.2.7.1 Low Pass Filter

The composite video output from V7 at 6V pk-pk is reduced to 3V pk-pk by R23 and R24 to form the input to the side chain low pass filter (LPF). Filtering is included to prevent the generation of spurious main clamp pulses by random noise and RF components carried by the input video.

The filter is formed by R116, R117, C45, C44, V45, which cuts off at approximately 1MHz. The cut-off frequency can be adjusted by C45 so that the filter's delay is as required for the correctly timed insertion of the regenerated sync pulses.

2.2.7.2 Sync Separation

Immunity to noise is further increased by ensuring that separation is at half sync amplitude. This is achieved by measuring peak amplitude in A4A, dividing by 2 with the potential divider R83, R79 and applying the resulting output as a reference voltage to the inverting input of the sync separator A4B, as shown in Figure 2-6. (See 2.2.9 for description of sync measurements).

2.2.7.3 Sync Blanking Generator

The sync blanking generator A2A to C lengthens the sync pulse so that when it is applied to V15 as a blanking pulse it starts before and ends after the incoming delayed sync pulse, thus ensuring that the latter is completely suppressed at the output.

2.2.7.4 Monostable Generation

The functions of the side chain are related to the separated sync pulses by means of monostable pulse generators, as shown by the waveforms given in Figure 2-6.

2.2.7.5 *Main Clamp Pulse Generation*

Monostable A3A is triggered on pin 4 by the separated sync pulse trailing edge and produces a 62µs positive-going output pulse (TP4). The leading edge of this pulse triggers the main clamp delay monostable A10A which produces a negative-going output pulse of duration variable up to 0.5µs.

A10B, the main clamp generator, is triggered by the trailing edge of A10A output pulse. However A10B output is inhibited by a pulse of 1.7µs duration from the monostable A9A which is triggered at the separated sync pulse leading edge.

The effect of A3A, A9A and A10A is to ensure that the 3µs main clamp timing pulse from A10B is delivered only during the back porch (see 2.2.8.2).

In the monostable A3A the negative-going output pulse (pin 7) is connected back to the negative-input trigger pin 5, thus preventing re-triggering of the monostable until 2µs before the trailing edge of the next separated sync pulse.

2.2.7.6 Main Clamp

The negative-going main clamp timing pulse (TP5) from A10B is applied to the composite MOSFET switch V13, V14. During the timing pulse V14 conducts, clamping the video input for V16 down to 0V during the back porch (see 2.2.6.3, Clamping Operation).

2.2.7.7 Side Chain Clamp

The side chain clamp timing pulse is generated by the 3µs monostable A3B which is triggered by the leading edge of A3A positive-going 62µs output pulse. V29 and V30 form a composite MOSFET switch in which V30 conducts during the side chain clamp timing pulse period.

The effect of the side chain clamp is to hold the output of the side chain low-pass filter V45 at 0V during the back porch, thus ensuring correct sync separation by A4A (see 2.2.7.2 Sync Separation)and ensuring consistent input sync pulse measurement by A4B (see 2.2.9.1, Input Sync).

2.2.7.8 Anti-lockout Circuit

A ‘lock-out’ condition exists if the sync pulse separator operates on a portion of the video waveform outside the sync period. To prevent this occurring the side chain includes an anti-lockout circuit.

This is basically a sync width measuring circuit which produces a logic ‘0’ when the input pulses are wider than 6µs, i.e. when the separated pulses exceed the normal sync pulse width of 4.7µs. Separated sync leading edges trigger the 6µs monostable A9B at Pin 5 and also provide the data input for the width discriminator, ‘D’-type flip-flop A7B, at Pin 5. A7B is clocked by the monostable output pulse.

When the separated train contains pulses wider than 6µs a ‘low’ is clocked through to the integrator A8. Broad frame pulses are clocked through as a result, and these are available at TP2. The integrator produces a logic ‘1’ when the input is a stream of broad pulses (or a continuous logic ‘0’ if there are no frame pulses present). The logic 1 activates the DC restorer V44, R111 until normal operation is restored.

Note:
The presence of broad pulses at the sync separator output indicates that the wrong part of the video waveform is being measured and that clamping is in the wrong place, as shown in Figure 3-8.

2.2.7.9 Sync Shaping Circuit

The sync shaper is used for re-insertion of sync pulses in NORMAL OPERATION (see. 2.2.2, Normal Operation). It is driven from the sync separator A4A via NAND Gate A2D, which can be used to switch off separated sync for either:

- measurement purposes, or
- in the AUTO sync mode, when the input sync level falls below -10dB of nominal value; this prevents spurious sync and noise being added to the video.

The sync shaper circuit V46/V47, and V51, is driven by the separated sync pulses, squared and inverted by A2D. The pulses are AC coupled by C29 and clamped by V55 with their lower level at -12V. V46 is interposed before V47, so that V47 conducts on low sync levels and V52 on high levels. V47 and V51 serve as charging paths, in opposite directions, for C49. When V47 conducts (leading edge) the voltage across C49 rises in an approximately linear manner until V48 conducts, clamping the level at 0V.

This level is maintained until V51 conducts (trailing edge) and V47 is switched off. C49 now discharges at a constant current until the voltage falls to -10V, clamped V53/R124. The process repeats for each sync pulse.

The charge and discharge currents for C49 are controlled by R121 (SET SYNC RISE) and R126 (SET SYNC FALL), thus providing slope adjustments of the leading and trailing edges of the regenerated sync pulse. At the junction of C49/R123 the output pulse is negative going between 0V and -10V. C50 rounds off the corners of the new pulses, to reduce the likelihood of ringing in later Exciter and Transmitter circuits. R46 controls the amplitude of the regenerated sync pulse for application to the sync - adding circuits, where the composite video signal is re-formed (see 2.2.6.6 Balanced/Unbalanced conversion and Sync Pulse reinsertion).

Rise and fall times are calculated as follows:

Charge on C49 = Q = CV = $I_o t$, where

I_o is the current generator output.

Change of voltage per second = $\frac{V}{t} = \frac{I_o}{C}$

If C49 = 220pF and I_o = 10mA, (nominal value),

therefore, rise time taken to change by 10V, i.e. rise or fall time, =

$$t = \frac{10}{10^{9}/22} = 220ns.$$

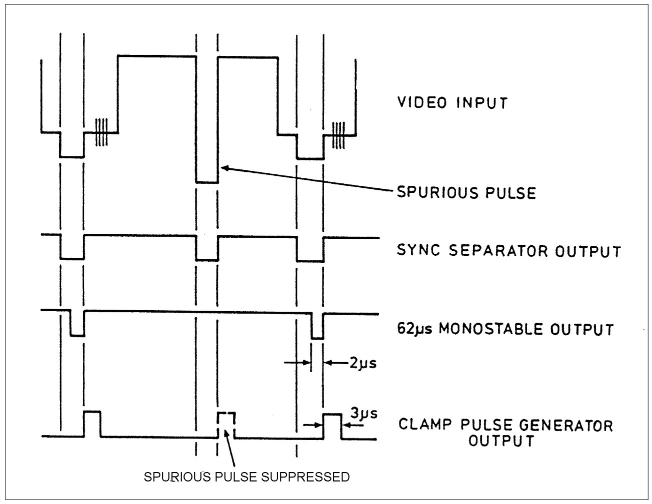


Figure 2-9 Spurious pulse suppression

2.2.8 Elimination of Spurious Pulses

2.2.8.1 Main Clamp

These are removed by the main clamp V13, V14, which is switched by pulses from the main clamp generator A10B.

There are several inhibiting circuits which make the clamp generation process immune to spurious pulses which would otherwise produce incorrectly timed clamp pulses. The clamp generator is inhibited for 62µs after the start of each clamp pulse in order to suppress any spurious pulses of short duration, as shown in Figure 2-9. The inhibiting signal is produced by a monostable in A3A, which is arranged so that it cannot be re-triggered.

2.2.8.2 Pulses in the Back Porch

Spurious pulses of less than 1.5µs duration are prevented from causing generation of clamp pulses and clamping to pulses occurring in the back porch, as follows. (see Figure 2-10). The monostable A9A is triggered from the leading edge of the separated sync pulse and produces negative-go-

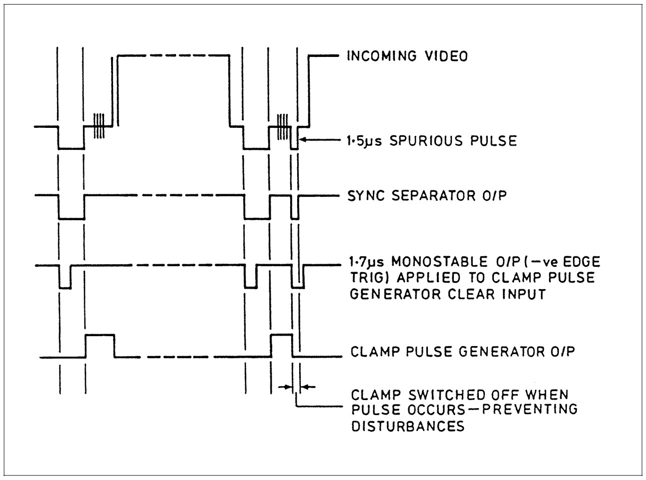


Figure 2-10 Prevention of clamp pulse generation

ing 1.7µs pulses which are connected to the inhibit input of the main clamp generator A10B at Pin 13. The main clamp generator is a monostable producing a 3µs pulse and triggered indirectly at Pin 12 via a single-shot monostable A3A, (the other pulse inhibiting circuit) and a 0.5µs delay generator circuit A10A. This delay compensates for the delay in the main video path less the sync separator response time.

The net effect is that the main clamp generator output is held high for 1.7µs after a negative-going edge (which may be a spurious pulse or sync) and does not produce a pulse until re-triggered.

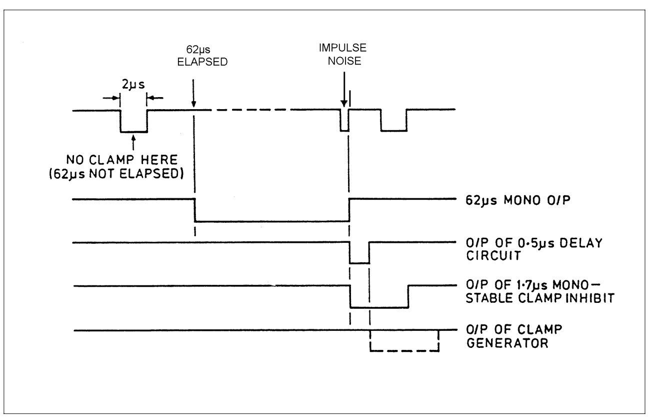


Figure 2-11 Equalising period suppression

2.2.8.3 Pulses in the Equalising Period

Spurious pulses occurring in the equalising period could create spurious clamp pulses which, if they occurred just before the 2µs narrow equalising pulses, could cause clamping to peak sync level. They are suppressed as shown in Figure 2-11.

The impulse shown is not a true impulse, as such a pulse would normally not get through the side chain low-pass filter preceding the sync separator.

Note:
If the clamp inhibit goes high again after less than the duration of a clamp pulse (assuming that a clamp is initiated while the inhibit is low) no residual clamp is generated.

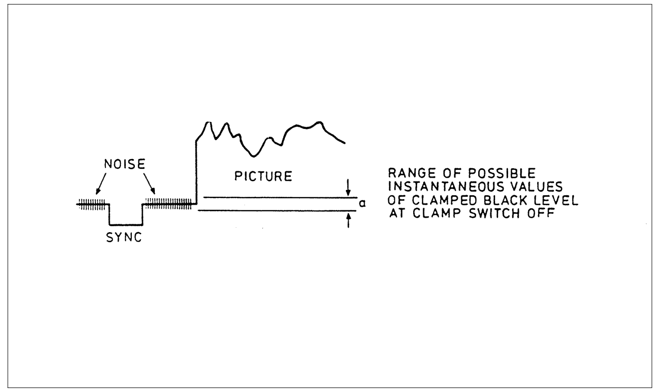


Figure 2-12 Noise conversion

2.2.8.4 Noise Conversion

Noise conversion occurs when a video signal of poor signal-to-noise ratio is clamped. In Figure 2-12, (a) is the range of possible instantaneous values of clamped black level at the time when the clamp is switched off. The clamp pulse may finish at any point in the noise waveform; the noise level clamped at that instant is then maintained for the whole line until the next clamp pulse arrives. This will create a new DC level for the following line.

The effect of this is that high-frequency noise above 15kHz is converted to low-frequency noise below 15kHz. This effect is reduced by including R28 in the main clamp path; it slows the response time of the clamp so that it is not able to respond to the rapidly changing noise waveform. However, as its value is increased, the hum rejection property of the clamp is reduced. A compromise is therefore chosen.

2.2.9 Sync Pulse Measurements

2.2.9.1 Input Sync

The low-pass filtered video output from V45 is clamped to 0V during the back porch by the side chain clamp (see 2.2.7 Side Chain), causing the sync pulses to be positioned with blanking level at 0V and sync tips at -0.9V (nominal). Measurement is performed in the peak rectifier circuit A46, V31, V32, R86, C34 and the sync tip voltage is stored by C34. The DC output is buffered by A5A and is fed as the reference input for the sync separator A4A via R83, R79. As the resistors are of equal value, the reference voltage stands at half-sync amplitude, enabling sync separation to be performed by slicing at that level (see 2.2.7.2).

The full rectified sync level output from A5A is also taken to the inputs of sync high/low comparators:

- A5B (sync high), where it is compared with a reference voltage of -1.6V, 4dB above normal sync level, derived from the potential divider R90, R91. The output is low for sync levels greater than -1.6V.
- A5C (sync low), where it is compared with a reference voltage of -0.3V, 10dB below normal sync level derived from R94, R95. The output is high for sync levels less than -0.3V.

The outputs of the two comparators are combined in A5D, which produces a low ‘go/no go’ logic signal to indicate when the sync level lies between -1.6V and -0.3V. The logic

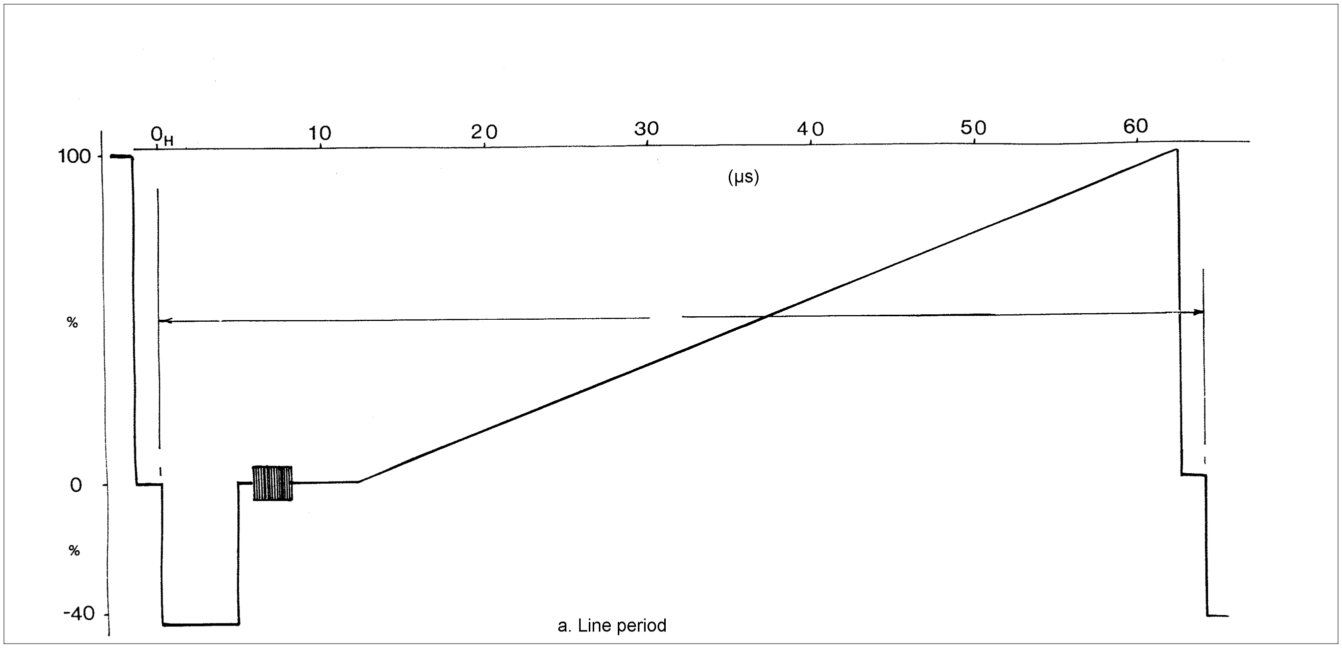


Figure 2-13 Details of line synchronising signals - line period

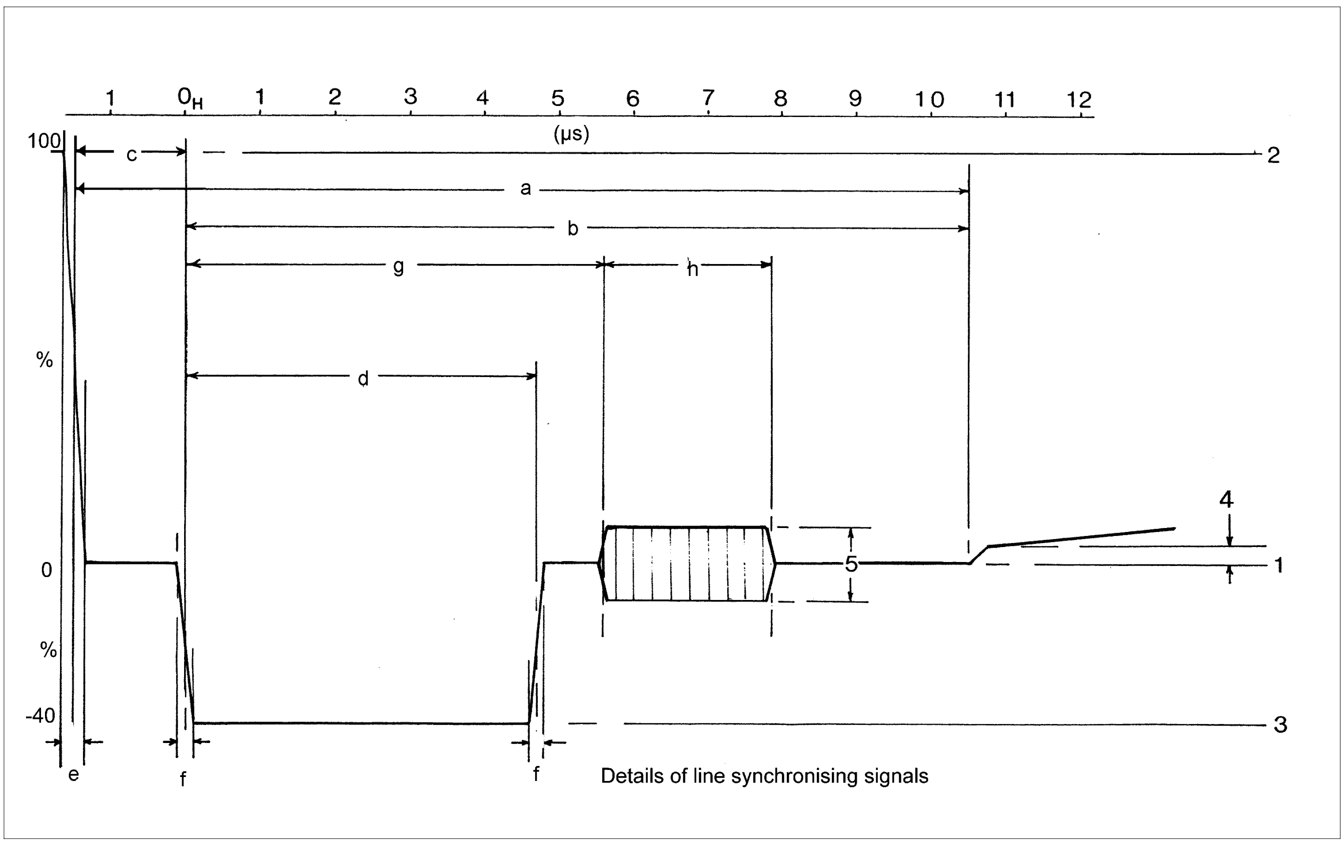


Figure 2-14 Details of line synchronising signals

signal drives the SYNC NORMAL LED H1 via V34 and V35.

Item	Characteristics
1	Blanking level (reference level) (%)
2	Peak White level (%)
3	Synchronising level (%)
4	Difference between Black and Blanking level (%)
5	pk-pk value of burst (%)
OH	Line period time datum (µs)
H	Nominal line period (µs)
a	Line blanking interval (µs)
b	Interval between time datum OH and back edge of line-blanking signal (µs)
c	Front porch (µs)
d	Synchronising pulse (µs)
e	Build-up time (10-90%) of the edges of the line blanking signal (µs)
f	Build-up time (10-90%) of the edges of the line synchronising pulses (µs)
g	Start of sub-carrier burst (µs) (after epoch OH)
h	Duration of sub-carrier burst (µs)

Table 2-1 Details of line synchronising signals (use in conjunction with Figures 2-13 and 2-14)

Note

Reference Table 2-1, all values are dependent on system in use.

The ‘sync low’ comparator output may also be used as the control input for the NAND gate A2D, when AUTO SYNC is selected, to inhibit generation of regenerated sync pulses when the input sync level is below -10dB. This prevents the insertion of spurious pulses when there is no sync input.

2.2.9.2 Output Sync

Output sync amplitude is measured by A6A at the composite video output, before the 75 ohm series resistor R72. At this point the amplitude is normally -0.6V. The measured level is compared in A6B with a reference of -0.3V, 6dB below normal; the comparator output drives V35 via V38. In normal operation with this arrangement the output sync measurement will override the input measurement, so that if output sync is too low H1 will not be lit even if the input sync level is satisfactory.

In the pulse mode, output sync measurement is inhibited by the removal of V37, so that H1 is illuminated to indicate correct input sync levels.

2.2.10 External Sync Application

In some applications there may be a need for an external sync pulse for use in associated modules including:

- Vision IF oscillator in which the IF is phase-locked to the line sync pulses.
- In pulser systems where delayed sync pulses are required for modulating the vision RF klystron beam current.

Early circuits include a pulser modification printed circuit board which delivers a positive-going sync pulse with blanking level at 0V and sync tips at +1V. The output of the sync high/low comparator circuit provides a low INHIBIT logic signal if the input sync signal is not of the correct amplitude. C29 is immobilised to inhibit the sync shaping circuits. Later circuits include a printed circuit board with remote ON/OFF switching for the sync pulses.

2.2.11 Setting-up Instructions

The following setting-up procedures are applicable to new untested units, or units which have been repaired following failure in service.

After completing the procedures the unit should be installed in the system and final adjustments carried out to meet the overall system requirements.

2.2.11.1 Test Equipment

- Power Supplies:
  1. +12V stabilised, 0.5mA
  2. -12V stabilised, 0.5mA
  3. +28V stabilised, 0.5mA.
- Digital voltmeter.
- Double beam oscilloscope with X10 probe.
- AF Signal Generator
- Video waveform generator.
- Waveform Monitor.
- 75 ohm return loss bridge.
- Measuring equipment for differential gain and phase.

2.2.12 Procedures

2.2.12.1 Output Amplifier Quiescent Current

a. Insert a resistor of initial value 39 ohms in the position of R70.

b. Connect a digital voltmeter or an AVO Model 8, set to 3V range, across R69.

c. Switch on and note the voltage across R69. It should be 1.0V ± 0.2V.

d. If the voltage is out of limits, increase the value of R70 if the voltage is too high, reduce it if it is too low.

2.2.12.2 Input Amplifier

a. Connect an oscilloscope through a X10 probe to the junction of R22, R23 (V6, V7 output).

b. Switch on and measure the DC voltage. It should be 0V ± 100mV.

c. Apply a common-mode AF signal to the amplifier input as shown in Figure 2-15.

d. Set R9 VIDEO GAIN to minimum gain (fully clockwise). This gives the amplifier a differential gain of approximately 3.2.

e. Adjust the signal generator to give 1.0V pk-pk at 50 Hz, as measured on the oscilloscope across R2.

f. Measure the 50Hz output at the junction of R22 and R23. This is a measure of the common-mode rejection ratio, which is given by:

$$\text{CMRR} = 20 \log 10 \left(\frac{Vin}{Vout}\right) + 10.1\text{dB},$$

where :

1. Vin = 1.0V pk-pk
2. Vout = measured pk-pk voltage.

   CMRR should be better than 35dB at 50Hz.

g. Repeat (e) and (f) at 10kHz. should again be better than 35dB.

h. Disconnect the AF signal generator.

i. Measure the return loss, using a 75 ohm return loss bridge. It should be greater than 40dB up to 6MHz.

Note

A good termination must be used.

j. Connect a video signal generator to X1 and set it to the multi-burst mode at a level of 1V pk-pk.

k. Connect the oscilloscope probe to the junction of R25 and C13 (V9 output).

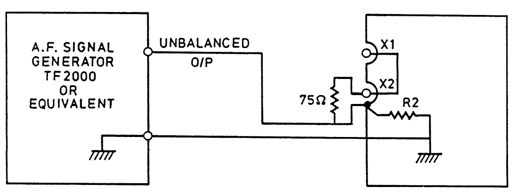


Figure 2-15 Application of Common-mode AF Signal

l. Adjust R9 to give a peak-to-peak video waveform of 3.3V (approximately 2.3V pk-pk picture).

m. Check that the 5.8MHz burst is not more than 0.6dB down (approximately 2.1V pk-pk).

n. Measure the peak-to-peak video signal at the junction of R118, C33 (V45 output). It should be 3.6V to 3.8V, of which the sync amplitude is 1.08V to 1.14V.

o. Measure the voltage at the output of the sync measuring circuit at the junction of R83 and A5 Pins 1, 2, using a digital voltmeter. It should be 1.08V to 1.14V.

2.2.12.3 Monostable Timings

Refer to section 2.2.7.4 and Figure 2-6.

a. Using a double-beam oscilloscope with a x10 probe, check the following pulses:

1. Output of the monostable A3A, at TP4; positive-going, 62µs ±0.5µs duration, triggered by separated sync pulse trailing edge. That is, there should be a negative pulse of 2µs ±0.5µs duration immediately before the end of the line sync pulse (ignoring frame pulses). If necessary alter the value of R77 to bring it within limits
2. The range of pulse widths available at the output of the main clamp delay monostable A10A. at pin 7; negative-going, duration variable from 0 to 0.5µs by means of C40, triggered by the leading edge of A3A output. Set it for 450ns ±10%
3. Output of the main clamp generator A10B, TP5; negative-going, 12V amplitude (ranging from 0V to +12V), 3µs ±.0.2µs duration, triggered by trailing edge of A10A output. If necessary alter the value of R115 to bring it within limits.
4. Output of the side chain clamp generator A3B at TP1; as for (c), adjust R78.
5. Output of the main clamp pulse inhibit monostable A9A, at TP6 ; negative-going, 1.7µs ±0.2µs duration, triggered by separated sync pulse leading edge. If necessary adjust R113.
6. Output of the lock-out detector monostable A9B, TP3; negative-going, 6µs ±0.6µs duration, triggered by separated sync pulse leading edge. If necessary adjust R112.

2.2.12.4 Clamps

a. Check that clamped video is present at the junction of C33 and R87 (SC CLAMP TC) and that the black level varies by less than 5mV from 0V with a bounce signal.

b. Set R87 to give 35dB of attenuation of the 50Hz hum when 0.5V of hum is added to the input video. If a source of hum is not available, set R87 fully anti-clockwise.

c. Using a double-beam oscilloscope, observe the main clamp pulses at TP5 and the sync pulses at R28/R27 junction; adjust C40 so that the pulse at TP5 occurs just after the trailing edge of the pulse at R28. (If possible make the clamp pulse straddle the colour burst.

d. Switch off and fit a temporary link in place of R28. Switch on and check for clamped video at the link.

e. Check the operation of the clamp: select a bounce waveform on the signal generator and check that black level does not vary by more than 5mV from 0V.

f. Remove the link and replace R28.

2.2.12.5 Sync Blanking and Balance-to-Unbalance Conversion

a. Switch off and fit a link between the common and OFF terminals of the sync mode selector (before A2D, pin 13).

b. Using a flat-field signal, monitor the waveform at the junction of R51 and R52 through a X10 probe. It should be non-composite video with blanking at 0V±100mV and peak white at +2.3V. This is the same as the picture amplitude at the clamp, i.e. 0.7 x 3.3V.

c. Adjust the offset null control R42 (BLANK STEP) to remove the step caused by offsets, and the spike cancelling trimmer C16 (SPIKE) to minimise the switching spike, as shown in Figure 2-16.

d. The dotted lines show incorrect adjustment of R42 and C16.

Note

This will require final adjustment at the unit's output after all the other adjustments have been made.

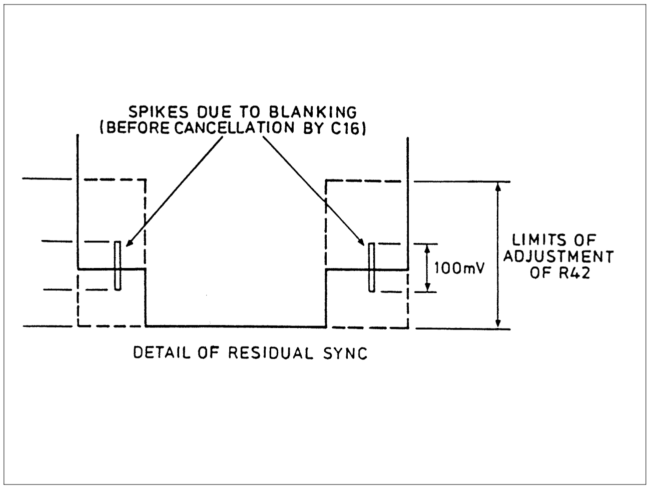


Figure 2-16 Minimisation of switching spike

2.2.12.6 Sync Pulse Shaping Circuit

a. Switch off and move the link to the ON position of the sync mode selector.
b. Set R46 (SYNC AMP) to minimum sync amplitude.

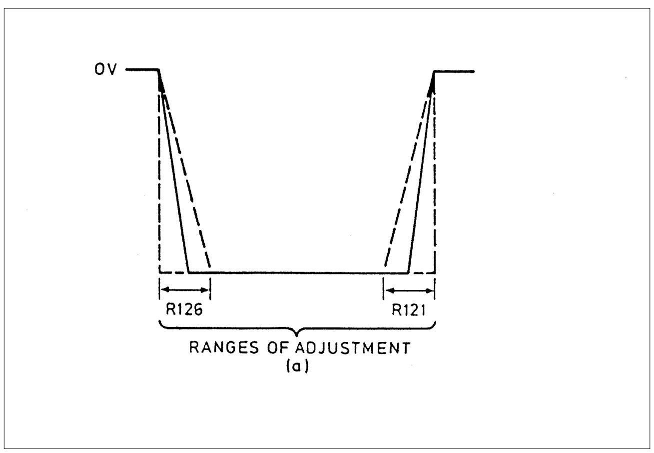


Figure 2-17 (a) Sync waveform

c. Switch on and monitor the new sync waveform at the junction of C49 and R123. It should be as shown at (a) in Figure 2-17.
d. Set the sync RISE (R121) and FALL (R126) times at the junction of R52 and R53 between the 10% and 90% points on the waveform, as shown in Figure 2-17(b), setting the sync amplitude by means of R46.
e. Adjust C50 SET SYNC SHAPE to just round the corners of the inserted sync pulse.

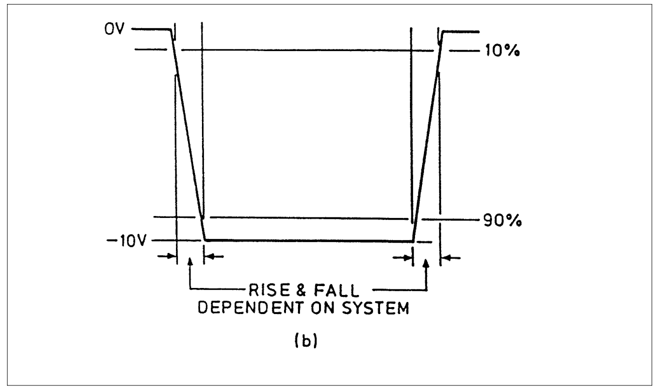


Figure 2-17(b) Sync waveform

2.2.12.7 Peak White Limiter and Output Stage

a. Connect a waveform monitor, e.g. TEK 1480, to the video output socket X4.
b. Check that a video waveform is present.
c. Check that the PEAK WHITE LIMITER R60 operates and that the limiting level can be varied from 0.25V to 1.1V pk-pk, measured at the module output. The latter value can be achieved by increasing video gain (R9).
d. Inject a staircase waveform with chroma and observe the differential gain and phase at the module output.
e. Tune L5 CHROMA PHASE for minimum change when the peak white limiter is made to operate.
f. Using a multi-burst signal, check that frequencies above 1MHz are not affected.
g. Set R9 (VIDEO GAIN) so that the video output is 1V pk-pk, with the limiter wound off.
h. Adjust C15 (HF ADJ) for equal amplitudes of all bursts, within ±0.25dB (±20mV).
i. Bar Tilt Compensation/HF Boost (separate PCB); Both Bar Tilt and HF Boost can be used together. If HF Boost only is required, turn off Bar Tilt by turning R2 fully anti-clockwise. If Bar Tilt only is required, turn off HF Boost by moving link X1 to the OFF position.
   1. For HF Boost adjust L1 for frequency and R1 for extent of lift. Adjust value of C1 for best boost compensation.
   2. Bar Tilt can be adjusted on final transmitter setting-up by means of R2.

2.2.12.8 Adjustment of Black Level Offset

a. Select a value for R130 to bring black level within ±5mV of 0V, after allowing 30 seconds for the unit to reach thermal stability.
b. Apply a staircase or ramp waveform to the input and, using a Vectorscope, overlay the input and output vectors.
c. Tune L4 MIN BURST PHASE for minimum phase error between the vectors.

d. Apply a composite trigger waveform and, using a double-beam oscilloscope, overlay the input and output video so that the sync pulses coincide.

e. Adjust C45 (DELAY) for minimum timing error between the trailing edges of the pictures.

The unit is now correctly set up and the overall tests can be carried out in accordance with the Video Processing Module specification.

2.3 Receiver Group Delay Assembly

2.3.1 General Description

Pre-correction for receiver group delay is applied to the processed video signal in a television transmitter drive/exciter system, to compensate for the group delay characteristics of domestic receivers. The group delay assembly contains a number of passive all-pass networks which can be varied to comply with different television receiver standards. A choice of one of seven predetermined group delay/frequency curves is available.

The circuit diagram for the assembly is given on drawing 3913 466 24810 Sh. 130-1.

2.3.2 Technical Data

a. Input Connector :
Type SMB

b. Input Impedance :
75 ohms

c. Return Loss :
Better than -26dB up to 5MHz

d. Insertion Loss :
Less than 0.2dB at 15kHz

e. Output Connector :
Type BNC

f. Output Impedance :
75 ohms

g. Amplitude/Frequency Response :
Within ±0.2dB from DC to 5MHz.

h. Group Delay/Frequency Response :
See Curves P1 to P7(Figures 2-18 to 2-24).

i. Dimensions :
310 x 140 x 37 mm.

j. Weight :
624 g. approximately

2.3.3 Technical Description

See circuit diagram 3913 466 24810 Sh. 130-1.

The Receiver Group Delay Assembly consists of a number of LC filters, which are adjustable for frequency and return loss characteristics. The number of filters and the values of capacitance and inductance of the required components vary according to the Group Delay curve appropriate to the required television standard.

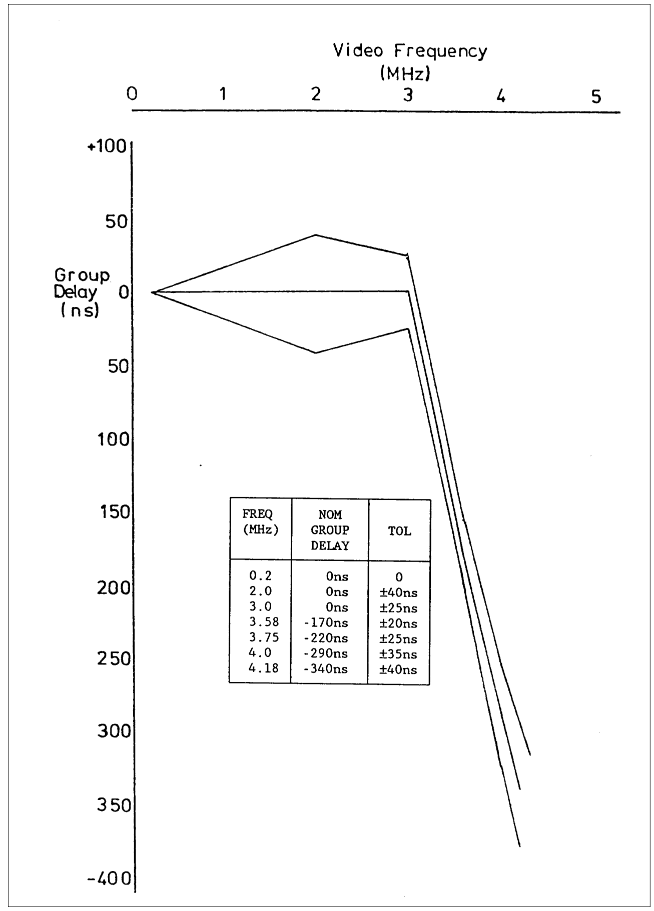


Figure 2-18 Receiver Group Delay Curve P1

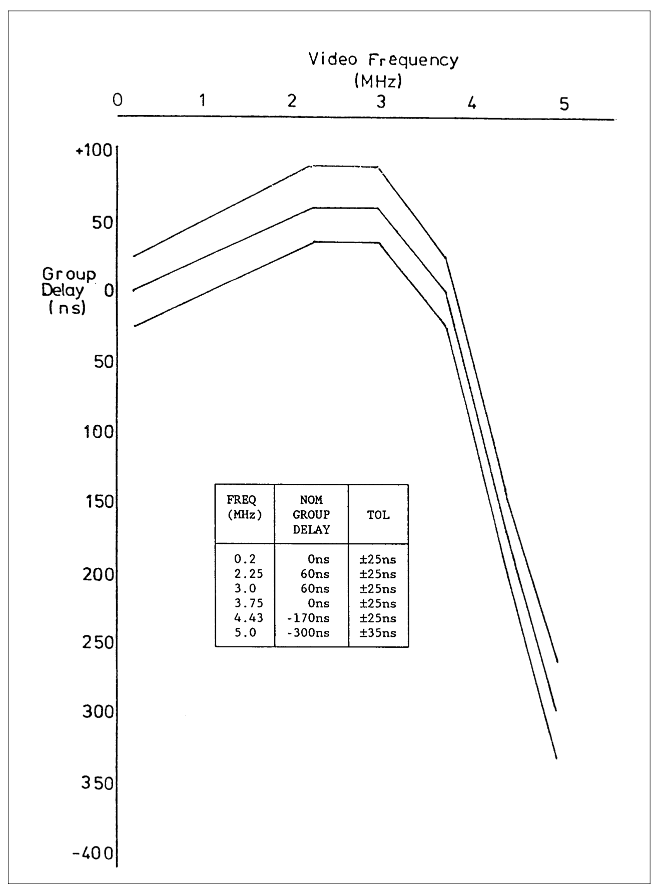
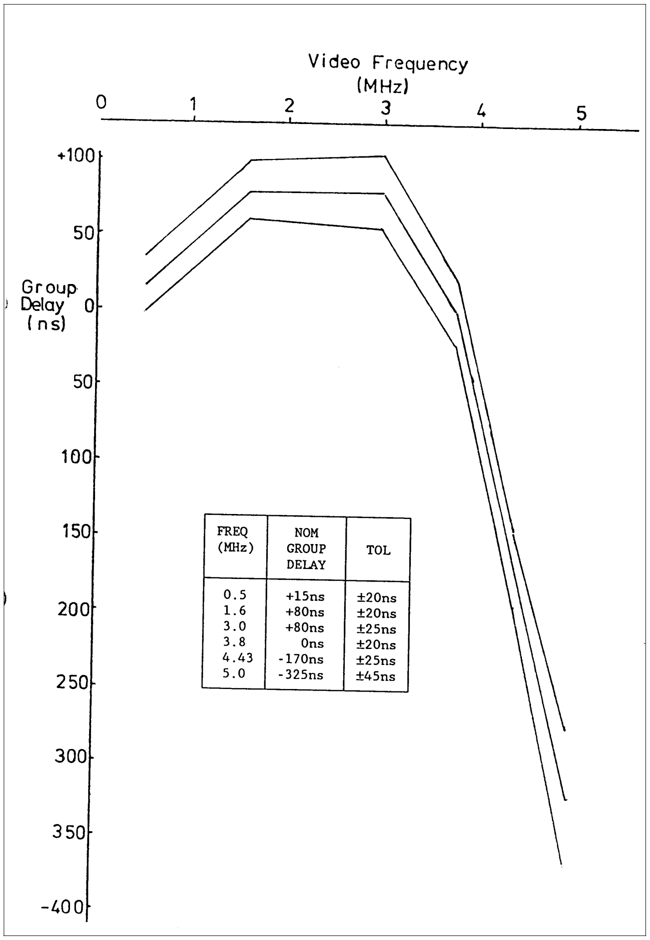
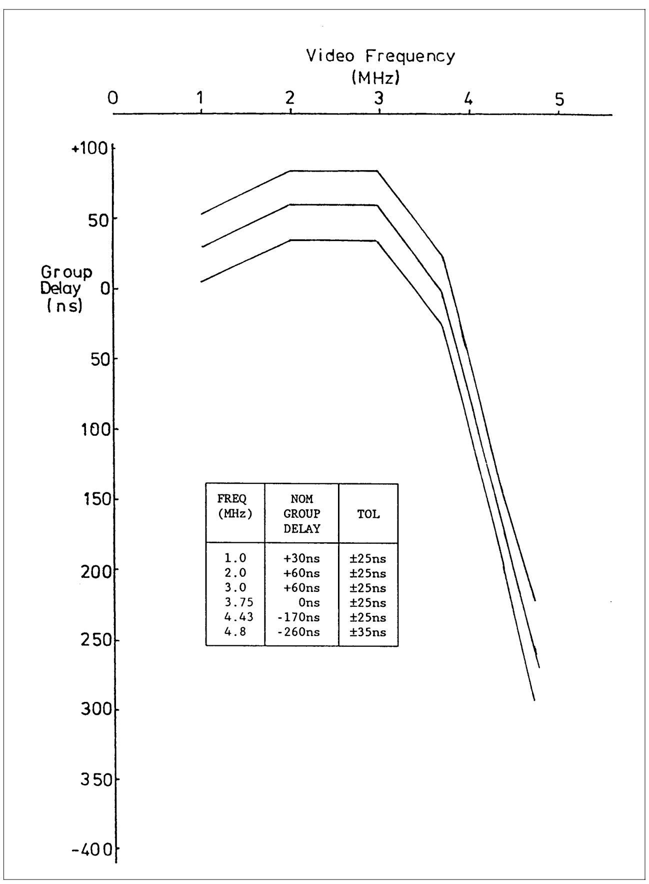


Figure 2-19 Receiver Group Delay Curve P2



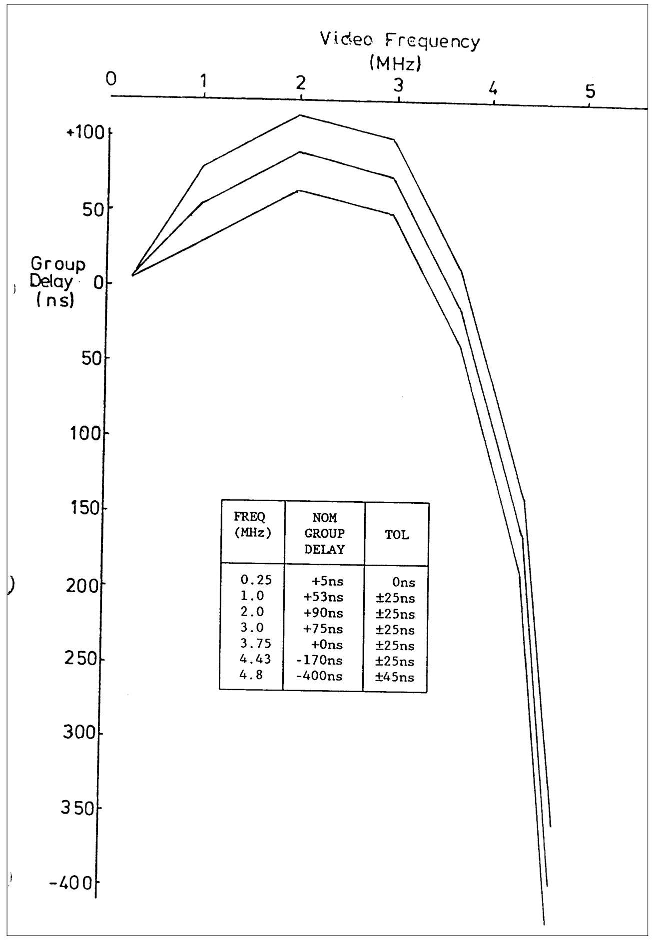
FREQ (MHz)	NOM GROUP DELAY	TOL
0.5	+15ns	±20ns
1.6	+80ns	±20ns
3.0	+80ns	±25ns
3.8	0ns	±20ns
4.43	-170ns	±25ns
5.0	-325ns	±45ns

Figure 2-20 Receiver Group Delay Curve P3



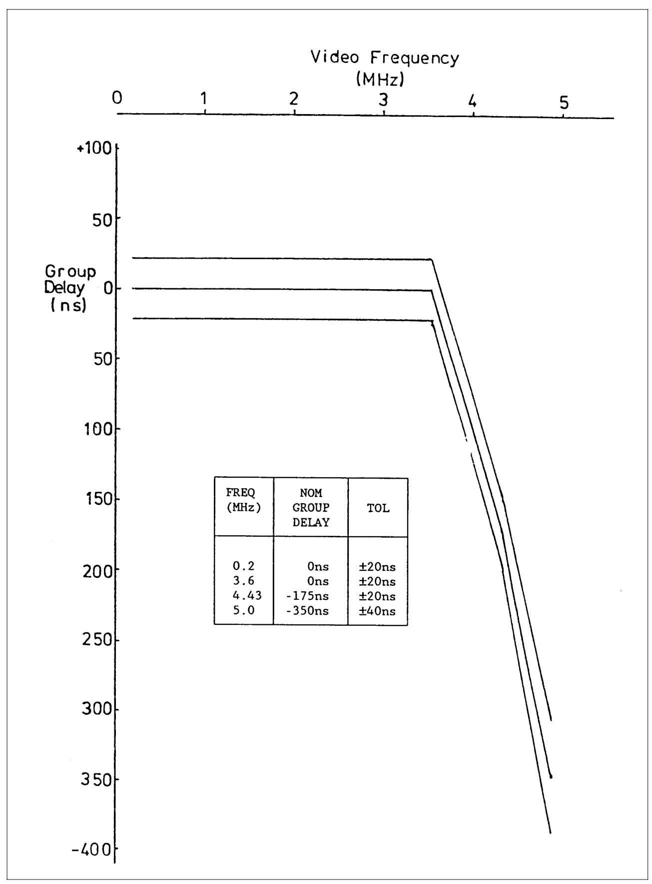
FREQ (MHz)	NOM GROUP DELAY	TOL
1.0	+30ns	±25ns
2.0	+60ns	±25ns
3.0	+60ns	±25ns
3.75	0ns	±25ns
4.43	-170ns	±25ns
4.8	-260ns	±35ns

Figure 2-21 Receiver Group Delay Curve P4



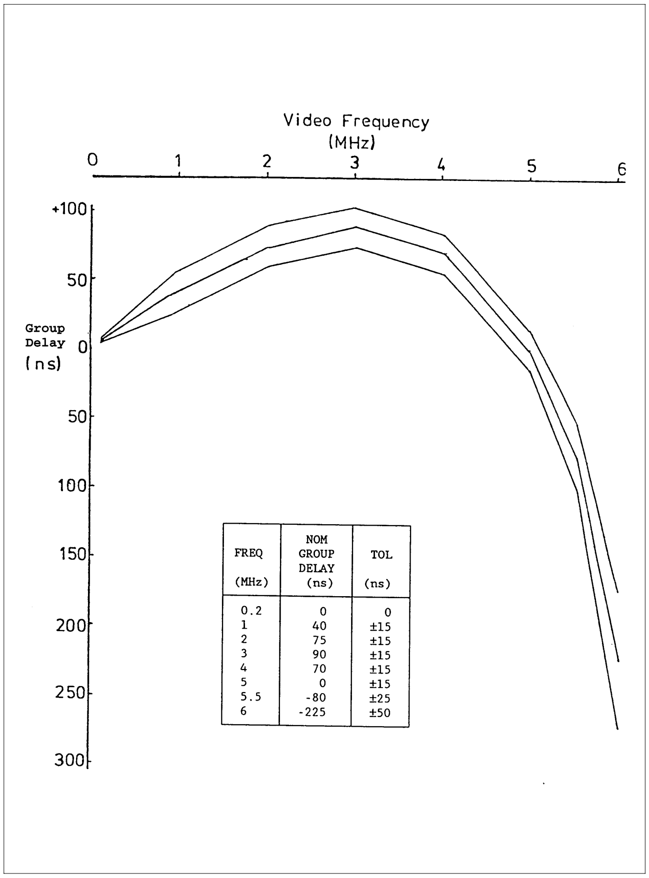
FREQ (MHz)	NOM GROUP DELAY	TOL
0.25	+5ns	0ns
1.0	+53ns	±25ns
2.0	+90ns	±25ns
3.0	+75ns	±25ns
3.75	+0ns	±25ns
4.43	-170ns	±25ns
4.8	-400ns	±45ns

Figure 2-22 Receiver Group Delay Curve P5



FREQ (MHz)	NOM GROUP DELAY	TOL
0.2	0ns	±20ns
3.6	0ns	±20ns
4.43	-175ns	±20ns
5.0	-350ns	±40ns

Figure 2-23 Receiver Group Delay Curve P6



FREQ (MHz)	NOM GROUP DELAY (ns)	TOL (ns)
0.2	0	0
1	40	±15
2	75	±15
3	90	±15
4	70	±15
5	0	±15
5.5	-80	±25
6	-225	±50

Figure 2-24 Receiver Group Delay Curve P7

To ascertain the component values for the different group delay curves, and their circuit references, parts lists 3913 466 709601 to 3913 466 709607 should be consulted.

To assist setting-up, the filter sections are connected to neighbouring filters by means of removable links. Each filter section is adjusted in isolation from all others, and the removable links permit test connections to be made only to the filter section under test. The maximum number of filter sections is six (for curves P5 and P7) and the minimum is four (for curve P1). Curves P2, P3, P4 and P6 utilise five filter sections. The output from the assembly is taken from the last filter section for each curve.

2.3.4 Setting-up Procedure

2.3.4.1 General

The setting-up of the assembly is performed by the adjustment of individual filter sections in isolation, commencing at the assembly input and working in sequence towards the output.

The adjustable elements consist of ferrite-cored coils, which are adjusted until the filter section exhibits the required frequency and return loss characteristics for the group delay curve under consideration. The two adjustments affect each other, so that the two processes are repeated for each filter section until the response is satisfactory.

Once each filter section has been set up it should not be further adjusted in an attempt to influence the overall response of the assembly.

A recommended sequence of operations is as follows:

a. Adjust the first filter section for the best return loss (minimum reflected energy).
b. Adjust the same section for minimum response at the specified frequency.
c. Repeat a. and b. until both responses cannot be improved.
d. In succession repeat the process for the remaining filter sections.
e. Re-connect all the inter-filter links.
f. Check the assembly as follows:
    1. Overall group delay conforms to the specified curve.
    2. Overall return loss is better than -26dB.
    3. The amplitude/frequency response is substantially flat over the video frequency range 0 - 5MHz.

If the assembly does not meet the required group delay curve, the individual filter sections should be re-checked.

2.3.4.2 Test Equipment

Test equipment is required as follows:

a. Sweep video signal generator
b. Video return loss bridge
c. Video CW signal generator (may be provided by 1)
d. Dual-channel 50MHz oscilloscope with X10 probes.
e. 75 ohm terminating resistor
f. 75 ohm resistor T-network
g. Video group delay measuring equipment
h. Frequency counter

The test equipment and filter section under test are connected for return loss and tuning adjustments as shown in Figures 2-25 and 2-26.

2.3.4.3 Procedure

(For new untested assemblies, or repaired assemblies).

a. Remove the outer cover from the assembly by taking out two screws on each side and two on the top, and lifting the cover clear of the assembly.
b. Remove all inter-filter links (see circuit diagram for references).
c. Connect a 75 ohm resistor between link terminals a and c, to terminate the first filter section.

Filter Section	1	2	3	4	5	6
Input	X1	b-c	e-f	h-i	k-l	n-o
Termination/Output	a-c	d-f	g-i	j-l	m-o	X4

Table 2-2 Filter Section Adjustments

d. Connect the test equipment to the first filter section, as shown for the return loss test.
e. Apply a swept video signal (0 to 5MHz) to the assembly input connector X1.
f. Adjust the ferrite cores of L1 and L2 to obtain the best return loss reading over the swept signal range on the oscilloscope display.

t. Remove the test equipment; replace the outer cover.
u. Record the assembly serial number and group delay curve number.

2.3.5 Test Configurations

Refer to Figure 2-25 and 2-26.

	Filter Section Adjustments					
Adjustment	1	2	3	4	5	6
Return Loss	L1	L5	L6	L8	L10	L12
Frequency	L2	L3/L4	L7	L9	L11	L13
			Tuning (MHz)			
Curve P1	1.2	2.025	3.055	3.88	-	-
Curve P2	1.32	2.025	2.90	3.78	4.87	-
Curve P3	1.36	2.025	2.825	3.75	4.52	-
Curve P4	1.315	1.95	2.80	3.75	4.35	-
Curve P5	1.215	1.51	2.30	2.95	3.56	4.33
Curve P6	1.265	1.89	2.86	3.72	4.57	-
Curve P7	1.36	2.025	2.94	3.87	4.90	5.90

Table 2-3 Filter Section Connections

Note:
The return loss will be between -32dB and -46dB.

g. Disconnect the return loss test equipment, and connect the filter section and test equipment for tuning adjustments.
h. Referring to Table 2-3, inject a CW video signal at the required frequency for the selected curve, and adjust L2 for minimum reading on the display.
i. Repeat steps c. to h. until no further adjustment is required for the first filter section.
j. Disconnect the test equipment from the first filter section.
k. Connect the test equipment to measure the return loss of the second filter section (see Table 2-3 for test connections).
l. Perform return loss and frequency checks on the second filter section until no further adjustment is required.
m. Carry out adjustments on the remaining filter sections until all individually require no further adjustment.
n. Remove the test equipment.
o. Re-insert the inter-filter links as shown on the circuit diagram.
p. Using the group delay test equipment, check that the assembly group delay over the video frequency range is within the limits for the required group delay curve.
q. Using the swept video input at X1, and taking the output from X4, check that the amplitude/frequency response is within ±0.2dB over the video frequency range.
r. Connect the assembly for an overall return loss test.
s. Check that the overall return loss is better than -26dB.

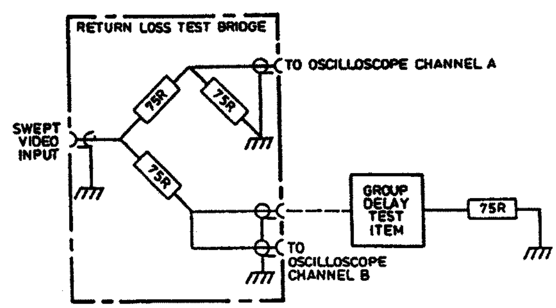


Figure 2-25 Return Loss Test Configuration

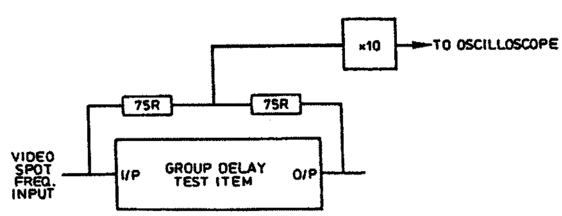


Figure 2-26 Tuning Test Configuration

2.4 Sound Modulator Assembly

2.4.1 Introduction

This module is designed for use in broad band television sound systems providing monophonic, stereophonic and Secondary Audio Programming (SAP) and professional channels, in which all the services modulate an FM subcarrier, as described in the BTSC system.

The module may also be used as a monophonic sound modulator as a 600-ohm balanced sound input is provided.

2.4.1.1 Audio

The audio outputs are selected internally by on-board links. Pre-emphasis is applied to the mono balanced sound input, the value being set at the factory to the system requirement. The MPX input is broad band, allowing the full BTSC signal to be applied. The SAP input allows a previously processed SAP signal to be added to either the MPX or balanced mono signal.

2.4.1.2 Intercarrier Frequency Modulation

Frequency modulation is achieved by applying the audio to a voltage-controlled oscillator (VCO) that has a rest frequency which is phase-locked to a crystal oscillator. The crystal frequency used will be the baseband sound carrier frequency, as defined in the particular television system specification, i.e. 4.5MHz, 5.5MHz, 6MHz or 6.5MHz. (See parts list and drawing Sh. 130-1 for details of versions).

2.4.1.3 Mixer and Output Stages

The output of the VCO is filtered and mixed with the external IF input in a double-sideband suppressed-carrier modulator. The lower sideband is filtered using a bandpass filter and presented to the IF amplifier and AGC section to give an output level of 0dBm into 50 ohms.

2.4.1.4 Automatic Gain Control

Part of the IF signal is rectified to provide a local AGC control voltage, and a switch selects either this or an externally generated voltage (provided from the demodulator which monitors the sound TX output level), thus giving LOCAL or AUTO AGC operation. The selected voltage is compared with an internally generated voltage and integrated to give the required loop gain and time constant characteristics.

The AGC voltage is applied to a P-I-N diode at the input of the IF amplifier, the effect being to regulate the RF gain of the amplifier in response to the AGC input. An AGC output is provided for metering.

2.4.1.5 Muting

A muting input, derived from the transmitter logic, is applied to a circuit which mutes the IF output when operated, reducing the output level. A red MUTE LED is illuminated when the mute is in operation.

2.4.1.6 Status Reporting

Status detection circuits are provided to monitor the VCO loop locking and to check that the IF output is above a preset threshold. When conditions are incorrect, RED LEDs are illuminated, accompanied by the requisite logic outputs to external control and monitoring equipment.

2.4.1.7 Construction

The electronic circuits are mounted on a printed circuit board, which is mounted in a standard case. Electrical and signal connections are made by plug and socket connections on the front. Access to preset circuit controls is obtained via holes in the top and side of the case.

2.4.2 Technical Data

2.4.2.1 Audio

a. Balanced Audio Input Level :
   Adjustable from 0dBm to+10dBm for ±50kHz deviation.
b. MPX Audio Input Level :
   5V p-p into 75 ohms for ±50kHz deviation.
c. SAP1 and 2 Audio Input Levels :
   5V p-p into 75 ohms for ±20kHz deviation.
d. Frequency Response :
   1. Balanced Input with Pre-emphasis IN:
      ±0.5dB, 30Hz to 15kHz. Relative to appropriate standard
   2. MPX Input, SAP Input and Balanced Input with Pre-emphasis OUT :
      ±0.2dB, 30Hz to 120kHz.
e. Audio CMRR :
   Equal or less than -45dB, 30Hz to 15kHz.
f. Sampled Audio Output (X7) ;
   2V p-p into 10k ohms, with balanced input at +8dBm.
g. Audio Distortion :
   Less than 0.1%, 30Hz to 15kHz,at ±50kHz or ±75kHz deviation.
h. Demodulated Output :
   0dBm into a 75-ohm load at ±50kHz deviation.
i. Frequency Response :
   ±1dB, 30Hz to 15kHz with appropriate de-emphasis.
j. Noise, Relative to ±50kHz Deviation:
   1. RMS 20Hz to 20kHz :
      Equal or less than -80dB
   2. CCIR Weighting:
      Equal or less than -70dB
   3. CCIR Weighting with de-emphasis (50µs) :
      Equal or less than -75dB
k. AM RMS Noise:
   1. Synchronous :
      Equal or less than -55dB
   2. Asynchronous :
      Equal or less than -65dB

2.4.2.2 Control

a. AGC Range :
   +2dB to -6dB minimum range.
b. External AGC Input :
   0 to 3V into 5 kilohms.
c. AGC Meter :
   Set at 3V ±0.2V for +2dB headroom.
d. External Power Control :
   0 to 5V into 10 kilohms.
e. Mute Input Threshold:
   1. Mute ON :
      +12V
   2. Mute OFF :
      less than 1V
f. Mute Impedance :
   Greater than 10 kilohms.
g. Muted IF Output :
   Less than or equal to 40dB below carrier.
h. Lock Status Output (Open Collector Circuit):
   1. In Lock :
      Input Resistance Low
   2. Out of Lock :
      Input Resistance High
i. Deviation Meter :
   Set at 2V for ±50kHz deviation.

2.4.2.3 Radio Frequency

a. Vision IF Reference Frequency :
   38.9MHz or 45.75MHz
b. Input Level :
   1mW into 50 ohms
c. IF Output Level (X1) :
   1mW
d. IF Output Level (X6):
   1mW ±1dB
e. Output Impedance : 50 ohms.
f. Spurious Outputs :
   Equal to or less than 65dB down on carrier.
g. Harmonic Rejection :
   Equal to or less than 40dB down on carrier.
h. Vision IF Rejection :
   Equal to or less than -70dB down on carrier.

2.4.2.4 Power Supplies

a. +12V :
   270mA
b. -12V :
   40mA
c. Consumption :
   3.7W (approximately).

2.4.3 Technical Description

Refer to the block diagram, 3913 466 37960 Sh. 136-1 and the circuit diagram, 3913 467 13940 Sh. 130-1.

2.4.3.1 Balanced Audio Input

R1 to R4 form a 1dB attenuator which presents a 600-ohm impedance to the balanced input at X10.

A1A is a differential amplifier, providing balanced-to-unbalanced conversion. R9 controls the inverting gain to set the common mode rejection ratio.

R10 sets the deviation, and C3/R11 forms a high-pass filter with a cut-off at 7.4Hz.

R157 feeds a sample of the unbalanced audio into X7, giving approximately 2V pk-pk for a balanced audio input of +8dBm.

A1B introduces pre-emphasis when C5 is grounded via an on-board link. The pre-emphasis time constant is set by R12/C5, and may be changed by altering the value of R12. R14 sets the upper frequency limit on the pre-emphasis to approximately 32kHz.

2.4.3.2 MPX and SAP Inputs

The MPX input at X8 is attenuated by R16 to set the deviation. Similarly, the SAP1 input at X4 is attenuated by R17 and the SAP2 input at X11 is attenuated by R165 to set the deviation.

2.4.3.3 Summing Amplifier

Any or all of the three audio inputs may be connected to the summing amplifier A2A via on-board links. The voltage gain of the SAP summing branch, given by R20/R19, is lower than the MPX or balanced audio branches to increase the sensitivity for setting a lower deviation.

A2B buffers the output of the summing amplifier for the phase-locked loop (PLL).

2.4.3.4 VCO and PLL

2.4.3.4.1 *General*

Frequency modulation is achieved by applying the audio signal to a voltage-controlled oscillator (VCO). The rest frequency of the oscillator is determined by a phase-locked loop, which locks the VCO to a crystal oscillator at the baseband sound carrier frequency, but allows the VCO to be modulated by having a low-pass loop filter with a very high time constant.

2.4.3.4.2 *Circuit Details*

A3A is arranged so that the output at A3 pin 1 is the sum of a DC voltage on A3A pin 3, which sets the VCO rest frequency, and the amplified baseband signal on A3 pin 2.

C100/L12 forms a low-pass filter, enabling the output at A3 pin 1 to pass to the VCO but blocking the frequency generated by the VCO going back to A3A.

The VCO is a Colpitts oscillator with C9/C10/L1/V2 as the feedback network and V1 as the amplifier. V2 is a variable capacitance double diode. Varying the reverse voltage on the cathodes varies the capacitance across them, controlling the oscillator frequency.

The signal is tapped from R28/R29, buffered by V4 and amplified to CMOS levels by A5A. Part of the output of A5A is further buffered by A5D and fed into A8 which is arranged as a 2^{14} divider.

The frequency that the VCO is to be locked to is generated by B1/C13/C14/C15 and A6. B1/C13/C14/C15 form a high-Q LC circuit which is driven by an invertor in A6 in a feedback loop to oscillate at the crystal frequency. This can be fine tuned by C15. A6 also divides the crystal frequency by 2^{14} for comparison with the VCO frequency.

The VCO and the crystal frequency, both divided by 2^{14}, are presented to the phase comparator of the phase-locked loop IC A7. If the signal frequency from the VCO is lower than the reference frequency, A7/13 will go from a high-impedance state to +12V in a series of pulses that will charge up C16 via R37 and C17 via R37/R38/R41.

Conversely, if the signal frequency from the VCO is higher than the reference frequency, then A7/13 will go from a high-impedance state to 0V in a series of pulses that will discharge C16 via R37 and C17 via R37/R38/R41.

Charging and discharging C17 increases and decreases the DC voltage on V2 cathodes via A3/3 which respectively increases and decreases the VCO frequency.

The dominant time constant in the loop filter is C17/(R38 + R37) which is approximately 100 seconds. This allows the VCO to be modulated by a baseband signal without the PLL trying to correct for it. The PLL will, however, correct for any long-term drift.

2.4.3.5 Out-of-lock Detection

Pin 1 of A7 is used to indicate whether or not the loop is in lock. The output at A7/1 consists of 0 to 12V pulses which can vary from having a very small mark/space ratio when in lock to having a very large mark/space ratio when out of lock.

This signal is presented to A12B, which inversely integrates the input when it differs from 6V. When in lock, A7/1 will be predominantly at +12V. A12B will integrate down via C25/R42 until it reaches a point close to the negative rail and saturates. When out of lock, A7/1 will predominantly be at 0V, therefore A12B will integrate up via C25/R43/V15 until it reaches a point close to the positive rail and saturates. The output of the integrator, whether low or high, is used to indicate if the loop is in lock or not. The different resistance paths ensure that the fast acquisition circuits are switched in quicker than they are switched out to ensure that any out-of-lock condition is re-tuned into lock.

2.4.3.6 Fast Acquisition and Mute Indication

A3B and A4D form a fast acquisition circuit for when the PLL is out of lock. When out of lock, A4/16 is high, which closes an analogue switch between A4/14 and A4/15. This switches in the unity-gain op-amp A3B which takes the voltage off C16 and bypasses R38 to feed C17 via R39/R41.

This has the effect of reducing the loop filter time constant from 100 seconds given by C17/(R37 + R38) to approximately two seconds given by C17/(R39 + R41), allowing the loop to quickly acquire lock.

A4A is an analogue switch which attenuates any baseband signal going into A3A while the loop is out of lock by shunting R40 with R21.

A4D takes the A12/7 output and, by switching R145 to ground feeds A21 to drive the LOCK LED.

A12A is a comparator whose output is integrated up or down instead of switched. When A12/7 is driven high, the voltage at A12/2 will be due to the voltage divider R34 and R46 and the forward conducting diodes V16 and V17. This causes A12/1 to be driven to the negative rail, and C26 to charge up. V19 clamps the voltage driving the muting circuits to -0.7V, which in turn mutes the IF output. Due to the action of the diodes V16 and V17, muting occurs quickly when an out-of-lock indication is given.

When the loop is in lock, and A12/7 is driven to the negative rail, C26 starts to discharge through R46 and R47. The voltage across V19 remains at -0.7V until the voltage at A12/2 reaches A12/3. It then increases to the normal unlocked level as the comparator switches states. The discharge of C26 ensures there is a delay in switching the mute off so that the IF output will always be presented to X1 in lock.

The output of A12/1 is also used to drive the MUTE LED via R142 and the high current transistor array A21.

2.4.3.7 Intercarrier Filter

A5E buffers the FM intercarrier from the PLL. This feeds a 1MHz bandpass filter L2/L3/L4 and C19/C21/R54 which is tuned at the intercarrier frequency. The filter reduces the high level of harmonics from A5E to present a clean intercarrier to the IF mixer via the buffer amplifier V7.

2.4.3.8 Mixer and IF Filter

A14 is configured as a double-sideband suppressed-carrier modulator. It receives an external IF frequency which is modulated with the FM intercarrier producing the desired lower sideband, a suppressed carrier which may be nulled by R72, and an unwanted upper sideband.

The mixer output is amplified by A15 and presented to the 4-stage high-Q 1MHz bandpass filter, which is tuned to the lower sideband. The filter performs the additional function of correcting for AM due to FM on a modulated carrier by adjustment of either L5 of L8. V5 buffers the filter in order to drive the IF amplifier section.

2.4.3.9 Internal AGC

V9 and A16 together act as a Voltage Controlled Amplifier (VCA). A16 has a fixed gain which is driven by the IF carrier that has passed through the P-I-N diode V9. The IF AC resistance of this diode depends on the DC current through it, which is supplied by the AGC circuit.

A sample of the output of this amplifier, A16/3, is buffered by V6 and fed to another amplifier A17. The output, A17/3, has two uses. It is used as the monitor output via the buffer V24, and is also rectified and smoothed by C46/V11 and V10/R101/C47 to give a DC level voltage, which is proportional to the output of A16.

A13A is configured as a constant voltage source by buffering the voltage across the zener diode V20. This provides a reference voltage via R59 for A13B. The DC level voltage is made to equal the reference voltage by the action of A13B. Any deviation by the level voltage from the reference voltage will cause C24 to charge in an opposite sense, hence altering the gain of V9 via R61/L15/R90 to correct the level voltage, i.e. if the IF carrier was to drop in amplitude from V5, then the rectified DC level voltage would also drop, causing C24 to charge up, increasing the voltage on R61. This in turn increases the current through V9 which lowers its AC resistance. The result is an increase in gain which compensates for the drop in signal.

R59 is usually set so that the VCA has +2dB of headroom.

The value of R61 may be changed to set the AGC metering voltage.

2.4.3.10 External AGC

The AGC may be connected to an external loop by changing on-board links to replace the reference voltage and the level voltage with their external equivalents through connections X5 Pin 10 and X3 respectively.

2.4.3.11 IF Out and Mute

The IF carrier from A16/3 is passed to the final amplification stage A18. The muting circuit is contained in this stage which comprises P-I-N diodes V14 and V3. These are capable of muting the carrier by 40dB when turned off.

The gain of this stage is set by R107 and R108 to give a power output of 1mW at X1.

2.4.3.12 Signal Status Indication

The SIGNAL STATUS LED indicates when the carrier is present at the IF output X1. It is extinguished automatically when the output is muted, by V26 connecting A21/6 to A21/3.

It is also extinguished if the carrier fails before the muting circuit by using the DC level voltage from the AGC circuitry as an indication of signal status. This is presented to the comparator A20 via R111/R112 which compares it to the threshold voltage set by R113/R114. In normal operation, when the carrier is locked or unlocked, the output A20/6 will be low with V25 ensuring that the comparator circuitry is effectively isolated from A21. If the IF CW fails, then A20 would be driven high, forward biasing V25 and extinguishing the signal status LED via A21/3.

The presence of a Sound IF signal at either C6 or C7 of the Auxiliary Signal Status printed circuit board will cause a charging of these capacitors to produce a HIGH at either of the inverting inputs of A1. Similarly, if the EXT MUTE signal is active (a HIGH) capacitors C6 and C7 will both be charged and produce a HIGH at both the inverting inputs of A1. The output from A1 under these conditions will therefore be a LOW at the output pin. (This signal is routed to the Sound Modulator Assembly Circuit where it is used to drive the green SIG STATUS LED indicator.

The signal is also buffered and output from the Sound Modulator Assembly Circuit via X8 as the SIG STAT signal).

2.4.3.13 Sound Demodulator

A5F buffers the FM intercarrier from the PLL to feed dual monostable multivibrator A9. A9 is configured as a non-retriggerable monostable multivibrator which is triggered on a high-to-low transition. This converts the frequency modulated signal to a signal which can be demodulated to baseband audio by integrating via C119/R126/C55.

The resulting signal is filtered by the Sallen and Key network on A10A, which filters out unwanted signals at intercarrier frequency. A10B amplifies and buffers the baseband signal which drives resistors R133 and R139, feeding the deviation meter and the de-emphasis circuit respectively.

The de-emphasis is introduced by A11A by the RC network R149/C54 in the feedback loop of the amplifier, and may be switched out by an on-board link disconnecting C54.

The de-emphasis may be altered by changing R149. The output at X2 is set by adjusting R139.

2.4.3.14 Deviation Meter

A11B amplifies the signal tapped from R133 and feeds a signal clamping circuit C73/V21, which clamps the most negative part of the signal to approximately -0.7V. V22/C59/R137 form a peak detection circuit whereby C59 is charged up to approximately the most positive point of the signal.

This voltage level is buffered by V31 to feed the deviation meter. The meter is calibrated at the maximum deviation by setting R133.

2.4.4 Testing And Setting Up

2.4.4.1 Procedures

It s assumed that the frequencies for vision and sound IFs are known before the tests commence, and that all links and test point connections are set as follows:

a. TP6 connected to TP7.
   TP8 connected to TP9.
   TP10 connected to TP11.
b. MPX link set to OUT.
   SAP1 and SAP2 links set to OUT.
   BAL link set to OUT.
   PRE-EMPH link set to OUT.
   DE-EMPH link set to OUT.
   AGC link set to EXT.
   PWR CONT link set to AUTO.

2.4.4.2 Electrical Checks

a. Connect the power supplies to the assembly under test and switch ON.
b. Check voltages and currents as follows:
   1. +12V at 270mA (approximately).
   2. -12V at 40mA (approximately).

c. Check that the voltage on TP4 is 10V±1V.

2.4.4.3 Lock Status

a. Adjust L1 until both LOCK and MUTE LEDs are extinguished. Adjustment should be made by turning the ferrite core of L1 one or two turns and waiting a couple of seconds to see if lock is achieved.

b. Check that the LEDs illuminate in the following sequence:

1. At switch on
   - both MUTE and LOCK LEDs illuminate.
2. After three seconds (approximately)
   - LOCK LED is extinguished.
3. After five seconds (approximately)
   - MUTE LED is extinguished.

c. Switch OFF.

2.4.4.4 Intercarrier Filter

a. With the module switched OFF, disconnect the links between TP6 and TP7 and between TP8 and TP9.

b. Connect the tracking generator via a 1k resistor to TP7, and the spectrum analyser to TP8. Switch module ON.

c. Tune the bandpass filter by adjusting L2, L3 and L4 until the following specification is achieved:
1MHz bandwidth ±100kHz at -3dB points centred on the intercarrier frequency.

Note:
As an aid to alignment the intercarrier frequency may be displayed on the spectrum analyser by temporarily shorting out TP6 and TP7.

d. Switch OFF. Remove all connections from the tracking generator and spectrum analyser to the module and replace the links between TP6 and TP7.

2.4.4.5 Carrier Null

a. Connect the vision IF to X9.

b. Switch ON and connect the spectrum analyser to the MON O/P on X6.

c. Adjust inductors L5 to L8 until the IF carrier frequency is clearly visible on the spectrum analyser. Its level should be between -40dBm and -70dBm.

d. Adjust R72 until the carrier reaches a minimum.

e. Switch OFF.

2.4.4.6 IF Bandpass Filter

a. Replace the link between TP8 and TP9.

b. Connect the power meter to X6 and switch ON.

c. Tune L5, L6, L7 and L8 so that the output power from X6 reaches a maximum (which should be greater than 1mW).

2.4.4.7 Fine Tuning of Sound Carrier

a. Connect a frequency counter capable of resolving down to 10Hz to X6.

b. Fine tune the sound IF by adjusting C15 (FREQ TRIM). The correct frequency may be calculated from:
sound IF = vision IF - crystal frequency.

2.4.4.8 Synchronous AM

a. Set the AGC link to INT and adjust R59 (INT AGC) until the power out of X6 reaches 1mW.

b. Remove the power meter and connect the modulation analyser to X6.

c. Connect the unbalanced audio input at 400Hz, 5V p-p to X8. Set the MPX link to IN and set the FM deviation to 50kHz by adjusting R16 (MPX).

d. Set the modulation analyser to measure synchronous AM. Adjust either L5 or L8 to achieve -55dB RMS or better (relative to 100% AM) of synchronous AM. If necessary adjust L6 or L7 slightly to achieve this figure.

e. Reconnect the power meter to X6 and set the AGC link to EXT.

2.4.4.9 IF Output, AGC and AGC Meter

a. Connect a 4k7 resistor between X5 Pin 9 and chassis earth.

b. Check that the sound carrier power level is between 1dBm and 3dBm. If necessary, increase R92 to reduce the gain or alternatively reduce R92 to increase the gain.

Note:
It may be necessary to change R140 in the above manner to 'fine tune' the level into the power range.

c. Connect the power meter to X1 and adjust R108 (SET OUTPUT LEVEL) until the sound carrier reaches 2dBm. If necessary, reduce R107 to raise the maximum power out of X1 over 2dBm, then set it to 2dBm by means of R108. In Version 6, connect a power meter to X11 and adjust R6 to set the output level to 2dBm. If necessary, adjust R5 to raise the maximum power output of X11 over 2dBm.

d. Set the AGC link to INT and adjust R59 (INT AGC) until the IF output level reaches 0dBm. In Version 6, with 0dBm set by R59, check that the X11 output is also 0dBm. Adjust R6 to set the X11 output to 0dBm if necessary.

e. Connect the power meter to X6 and check that the output lies between -1dBm and +1dBm.

f. Set the voltage across the 4k7 external resistor on X5 Pin 9 to 3V ±2V by altering the value of R61. To increase the voltage, increase the resistance.

g. Check that the output(s) of X1 is still 0dBm. If it has changed, then repeat (b) to (f) above.

h. Connect the power meter to X6 and check that the output lies between -1dBm and +1dBm.

i. Using the spectrum analyser, check that the outputs of X1, X6 and X11 meet the following specification:

1. Harmonics less than 40dB below carrier for outputs at X1 and X11.

2. Harmonics less than 35dB below carrier for output at X6.
3. All spurious less than 65dB below carrier.

Note:
Adjust L2 slightly, if necessary, to clear spurious next to carrier.

2.4.4.10 Distortion Setting

a. Connect the FM/AM demodulator to the IF output connection X1 and set up for FM deviation measurement. Connect the distortion/noise meter set with a bandwidth of 10Hz to 20kHz to the demodulator.
b. Connect the unbalanced audio signal at 400Hz, 5V p-p to X8.
c. Adjust R16 (MPX) until the deviation is set to ±50kHz and calibrate the deviation meter to 100%.
d. Adjust L1 until the distortion reading reaches a minimum. If the deviation changes slightly then reset using R16 (MPX). The final distortion reading should be less than 0.1%.
e. Vary the audio input over the frequency range 30Hz to 15kHz and check that the distortion is better than 0.1%.

2.4.4.11 Bandwidth and Noise

a. Set a 0dB reference on the distortion/noise meter for ±50kHz deviation.
b. Vary the audio input over the frequency range 30Hz to 120kHz and check that the amplitude response is flat ±0.3dB.
c. Remove the audio input.
   1. Check the FM noise as follows:
   2. With 20Hz to 20kHz bandwidth, equal or less than -80dB RMS.
   3. CCIR weighting, equal or less than -70dB.
d. CCIR + de-emphasis (50µs), equal or less than -75dB.
e. Relative to 100% AM check that the RMS asynchronous AM is equal to or less than -65dB.

2.4.4.12 Audio Levels

a. Set the AM/FM demodulator to measure FM deviation.
b. Connect the unbalanced audio input at 400Hz, 5V p-p to X4. Set the SAP1 link to IN.
c. Set the SAP1 deviation to ±20kHz by adjusting R17 (SAP1).
d. Remove the unbalanced audio input from X4 and connect it to X11. Set the SAP2 link to IN.
e. Set the SAP2 deviation to +20kHz by adjusting R165 (SAP2).
f. Remove the audio input from X11 and connect it to X8. Set the deviation to ±50kHz by adjusting R16 (MPX).
g. Remove the audio input from X8 and connect the balanced audio input at 400Hz +10dBm to X10. Set the BAL link to IN.
h. Set the deviation to ±50kHz by adjusting R10.

2.4.4.13 Common Mode Rejection Ratio

a. Connect the FM/AM demodulator to X1.
b. Connect the audio distortion/noise meter to the demodulator audio output and set up for 0dB reference at ±50kHz deviation.
c. Disconnect the audio input from X10.
d. Using an audio input connector with both live lines connected together, apply the audio signal used in (b) between the ‘hot’ lines of X10 and 0V.
e. Adjust R9 (SET CMRR) for minimum reading, and check that this is equal or less than -45dB over the audio input range 30Hz to 15kHz.

Note:
The CMRR can be monitored on a scope on the AF output of the demodulator or on TP1 on the board.

f. Restore the X10 audio input connections to balanced and apply a 400Hz, +10dBm audio input signal.
g. Reset R10 (BAL) to obtain ±50kHz deviation.

2.4.4.14 Pre-emphasis

a. Set the PRE-EMPH switch to IN.
b. Set the balanced audio input level to 0dBm, at the reference frequency as follows:
for 75µs pre-emphasis - 8.2kHz,for 50µs pre-emphasis - 12.3kHz,and at a 0dB reference on the distortion/noise meter.

	dB	**75µs**	**50µs**
	3.0	11.7kHz	17.7kHz
	0.0	8.2kHz	12.3kHz
	-3.0	5.6kHZ	8.4kHz
Reference	-6.0	3.7kHz	5.5kHz
	-9.0	2.1kHz	3.2kHz
	-11.5	740Hz	1.1kHz
	-12	100Hz	100Hz

Table 2-4 Distortion/Noise meter readings

c. Refer to the table below and check that the distortion/noise meter readings agree to within ±0.5dB of the amplitude levels shown.

2.4.4.15 Lock Status

a. Connect the +12V supply via a 1 kilohm resistor to X5 Pin 8.
b. Check that when locked, the voltage on X5/8 is less than 0.1V and when out of lock, the voltage on X5/8 is +12V.
c. Disconnect the resistor and the +12V supply.

2.4.4.16 External Mute

a. Connect the spectrum analyser to X1 and the +12V supply to X5/1.

b. Check that when +12V is applied, the output signal is muted by at least 40dB, and when 0V is applied to X5/1, the output signal returns to 0dBm.

2.4.4.17 Demodulated Audio Output

a. Connect the FM/AM demodulator to the IF output connection X1 and set up for deviation measurement. Connect the balanced audio input at 400Hz, +10dBm to X10 and check that the deviation is set at 50kHz.

b. Connect a 75-ohm resistor to X2 and, using a DVM, set the demodulated output to 0.273V RMS (0.77V p-p) by adjusting R139 (in effect, setting a 0dBm level on a 75-ohm load).

2.4.4.18 Demodulated Audio De-emphasis

a. Decrease the balanced audio input to 0dBm and link IN the pre-emphasis. Adjust the audio input so that the deviation reads ±50kHz at 15kHz.

b. Link IN the demodulated audio de-emphasis.

c. Connect the distortion/noise meter to X2 and set a 0dBm reference.

d. Vary the frequency from 15kHz to 30Hz and check that the demodulated output stays within ±1dB of the 0dB reference.

2.4.4.19 Deviation Meter

a. Connect a 4k7 resistor between X5 Pin 11 and chassis earth.

b. Set for ±50kHz deviation at 1kHz.

c. Adjust R51 (meter) until the voltage across the resistor is 2V.

2.4.5 Sampled Audio Out

a. Connect the balanced audio input, set to +8dBm at 1kHz, to X10.

b. Check that the voltage at X7 is 2V p-p ±0.5V.

Note:
If any other voltage is required from X7, then the input attenuator R1 to R4 will need to be altered.

2.5 Video Corrector, Modulator and SAW VSB Filter Assembly

2.5.1 General Description

This assembly accepts a video signal and an intermediate frequency signal at X1 and X2 respectively. Within the assembly's circuitry precorrection of the video is performed, together with amplitude modulation of the vision intermediate frequency signal. These signals are then filtered in a surface acoustic wave (SAW) filter to obtain the required bandpass VSB response.

Three main functions are performed on the printed circuit board. They are:

a. precorrection of the video signal

b. modulation

c. VSB filtering

The assembly is provided with input and output coaxial connectors which, together with suitable internal linking, allows testing of several functions. Tested are the precorrection and modulation sections, and the VSB filtering section, either of which can be tested individually or can be bypassed.

The circuit requires an IF input of 1mW and a video input of 1V to produce an amplitude modulated output of 1mW peak sync. Preset controls allow modulation depth and output level to be set to suit system requirements.

Correction can be made selective and affects either luminance and chrominance or luminance only. Automatic Gain Control is provided in order to keep the modulation depth constant during the time of adjustment.

The VSB filter section has unity gain over the pass band and is fitted with an appropriate SAW filter to suit system requirements. The SAW filter is temperature controlled by an oven.

2.5.2 Technical Data

a. Video Input :
1 V pk-pk with blanking level at earth potential. 75 ohms. SMB connector.

b. Vision IF Input :
1 mW in 50 ohms. SMB connector.

c. Vision IF Input VSWR :
Less than 1.2.

d. Vision IF Output :
1 mW peak sync nominal, adjustable. 50 ohms. MB connector.

e. Frequency response :
   1. No correction applied:
      flat within ±0.1dB.
   2. With correction :
      flat within ±0.3dB.

f. Vision IF Output VSWR :
Less than 1.2.

g. No Correction :
LF linearity <2%,
Diff Gain < 2%,
Diff Phase < 2°

h. Maximum Correction :
LF linearity, 12%;
Diff Gain, 3%;
Diff Phase, 5 degrees.

i. Power requirements :
   1. Modulator :
      +12V 280 mA approximately,
      -12V 170 mA approximately.
   2. Oven :
      +12V 350 mA approximately.

j. Operating Temperature :
   10 to +70 ° C.
k. Oven Temperature :
   +75 ° C nominally.
l. Dimensions.:
   Width, 37 mm ; Depth, 310 mm; Height, 140 mm.
   Weight : approximately 700 g.

2.5.3 Technical Description

Refer to schematic 839 8121 555.

The video signal is input at X1 then processed by operational amplifier A7A. The gain of A7A is increased when diode V21 becomes conductive, i.e. when the signal is above the threshold determined by R53 (ONSET). The amount of gain increase is set by R66 (SLOPE). L5, C29, R76, form a notch filter tuned on the chrominance subcarrier. This allows correction to either affect luminance (low frequency) only or luminance and chrominance, depending on the setting of R76 (CHROM REJECT).

FET V19 is voltage controlled and sets the linear gain of A7A. V19 is controlled either by a regulated voltage set by R65 (MANUAL GAIN), or automatically by an AGC loop. The AGC loop is made by setting link LK3. AGC should be used when setting the best linearity and with a staircase video waveform only.

V22 and C34 form a detector which feeds the AGC loop amplifier A7B, the gain of which is determined by R58 and R56.

The video signal is then fed to the double sideband modulator A1, with the IF carrier being fed via amplifier V6.

The DSB signal at V12 can be linked to an output for external use. For normal operation LK2 is set in the a-b position and the DSB signal is fed to A4, the SAW VSB filter. The characteristics of this filter are chosen to suit the television system in use.

R75 (VIDEO BIAS) sets the operating point and therefore the depth of modulation, while

R42 (SET GAIN) adjusts the gain of A2, which sets the DSB output level at X7. R32 (select on test) sets the gain of A3, making the output level at X4 the same as X7, i.e. unity gain through the final section. The output is detected by V2, V3 which switches on LED H1 when the signal is present.

A VSB sweep input is provided at X3 to allow the characteristics of the SAW filter to be measured using IF sweep techniques.

When used on System I and System M equipment the SAW filter A4 is held at a constant temperature of nominally 70°C by a simple oven arrangement. Temperature sensor V4 and heating transistor V5 are mounted on a heat sink situated on top of A4. A5 switches V11, V5 on and off depending on the ratio of resistance between R4 and R33. Refer to the parts list for details on filters and ovens.

2.5.4 Test Procedure

a. Connect the power supplies and check the current consumption. It should be as follows:
   1. +12V:
      280 mA
   2. -12V:
      170 mA
b. Connect +12V to the oven supply and check the current consumption. It should be approximately 350mA and LED H2 should be OFF.
c. When H2 comes on, the oven should have reached a temperature of approximately 75°C. This temperature should be maintained to within ±3 °C as the oven circuit cycles on and off.
d. Turn all potentiometers counter clockwise. Set link LK 3 to MANUAL. Connect a staircase video waveform on X1.
e. With an oscilloscope check the waveform at TP1. White level should vary from approximately 0.9 to 1.2V when turning MANUAL GAIN clockwise.
f. Set link LK3 to AGC. The ONSET and SLOPE potentiometers being turned fully counter clockwise, the white level at TP1 should be 1.2V ±0.1V. If not, adjust R78.
g. Turn SLOPE fully clockwise and check that when turning ONSET, the waveform at TP1 is bent but the white level remains constant.
h. Reset ONSET and SLOPE fully counter clockwise. Set link LK 3 to MANUAL and adjust MANUAL GAIN so that the white level at TP1 is the same as that when in AGC.
i. Connect an IF carrier signal source, suitable for the system in use, at 0dBm to X2 (IF CW INPUT).
j. Set link LK1 in the a-b position and link LK2 in the ‘b-c’ position (DSB configuration).
k. Apply a staircase video signal to X1 (VIDEO INPUT), and connect an oscilloscope of 60MHz bandwidth, terminated in 50 ohms, to X7 (DSB OUTPUT).
l. Check that an amplitude-modulated signal is present at X7.
m. Adjust R75 (VIDEO BIAS) to obtain zero cross-over (i.e. 1% residual carrier). This checks the modulation capability. Then re-adjust R75 to obtain the required depth of modulation for the system in use, i.e. 12.5% for system M.
n. Remove the video input from X1 and terminate X1 in 75 ohms.
o. Remove the oscilloscope from X7 and replace it with a power meter.
p. Adjust SET GAIN for black level output power appropriate to the system.
q. Reconnect the oscilloscope, terminated in 50 ohms, to X7 and the video signal to X1.
r. Recheck the modulation depth.
s. Check that the luminance and chrominance gain are equal. If not adjust C50 (on tags).
t. Disconnect the video signal, terminate X1 in 75 ohms, set link LK2 in the b-a position (VSB CONFIGURATION).
u. Connect a power meter to X4 (VSB OUTPUT).

v. Select a value for R32 which gives the required black level output power.

w. Check that H1 is illuminated and that it extinguishes when carrier is removed.

x. Connect the VSB output to a demodulator. Connect a 10-steps staircase with chrominance on X1 and observe the demodulated IF with a vectorscope.

y. Set ONSET and SLOPE fully clockwise. Set CHROM REJECT at the centre of its range. Then adjust inductor L5 so that differential gain is minimum. If L5 is out of range then adjust C29.

z. Remove all correction: ONSET and SLOPE fully counter clockwise. Let CHROM REJECT at the same position (centred).
Check that :
   1. luminance linearity; <2%
   2. differential gain; <2%
   3. differential phase; <2 %

aa. Re-check power levels and modulation depth and confirm that the frequency response is in accordance with the system requirements.

2.6 Differential Phase Corrector

2.6.1 General Description

2.6.1.1 Differential Phase

Differential Phase Correction is applied to the VIDEO signal supplied to the Vision Modulator, not to the modulated IF as in previous correctors. This is achieved using an 'Elastic Delay Line', in which the required phase changes are produced by creating a variable delay as a function of picture luminance level. The polarity and law of this delay is variable, thereby allowing correction of different amplifier phase distortion characteristics.

2.6.1.2 Carrier Phase

Carrier Phase correction is applied to the IF CW signal prior to vision modulation (previous correctors operated on the modulated IF signal). The same video signal is used to drive the corrector as for differential phase. Separate Video processing circuits are used, offering the same shape generation as for differential phase.

A phase-shifting network is used which creates little amplitude modulation.

A delay line is fitted in the main video output which is adjustable so that the carrier phase modulation is correctly timed relative to the amplitude modulation present at the output of the vision modulator. This correctly phases the sidebands produced by phase modulation with those generated in the vision modulator. In this way a flat frequency response is obtained within the double sideband portion of the transmitter swept response.

2.6.2 Technical Data

a. Video Input :
7V Peak White, Black Level 0V, Sync -0.3V (if required).

b. IF Input :
1mW CW

c. Video Output :
0.7V Peak White, Black Level 0V, Peak Sync -0.3V.

d. IF Output :
1mW CW

e. Impedances:
IF :
50 ohms,
Video :
75 ohms

f. Maximum Correction :
Differential Phase :
More than ±45°.
Carrier Phase :
More than ±20°.

g. LF Non-linearity:
Less than 2%, with correction off.

h. Differential Gain :
Less than 2%, with correction off.

i. Video Frequency Response :
DC to 5.5MHz ±0.5dB, with correction off.

j. Group Delay :
Less than 50ns.

2.6.3 Technical Description

2.6.3.1 Differential Phase

V1 and V2 are complementary emitter followers which form a buffer for the video signal feed to the distortion generating circuits, introducing no black level offset. Video is applied direct from the input via R115 to the inverting and non-inverting delay line drivers.

V7, 8, 9 and 10 form an inverting buffer with unity gain and no shift in black level voltage. V10 is a current generator, V9 a voltage amplifier and V7 and 8 a long-tailed pair (differential amplifier). Together they form an operational amplifier.

V11, 12, 13 and 14 form a non-inverting video buffer with unity gain; the circuit operation is as for the inverting buffer.

The two buffers described produce balanced video with black level at zero volts and peak white at ±1V, i.e. 2V peak white to peak white.

The balanced video drives a balanced Elastic Delay line formed by L3 - 14 and V24 - 29 which are double varicap diodes. The delay through the line is a function of the diodes' capacitance and therefore is variable by the reverse voltage applied via R64. Note that if the line were not balanced, the delay would also be a function of the throughput video white level. Using positive and negative video in this way and converting back to unbalanced video, any delay variation caused by picture level (while the voltage across C22 is held constant) is cancelled out. The delay and hence subcarrier phase is therefore only a function of the voltage across C22.

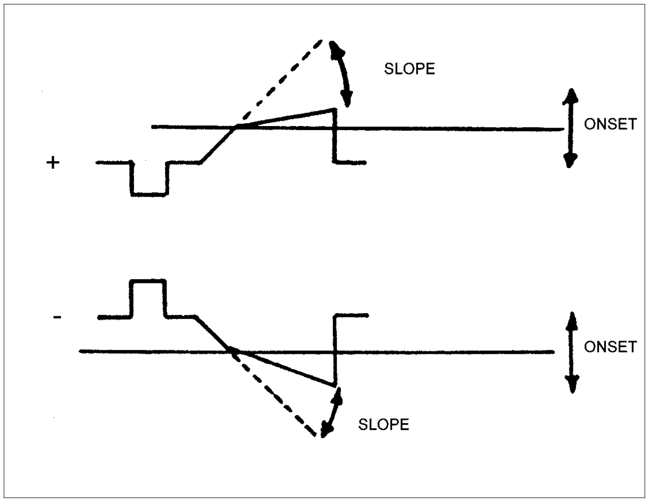


Figure 2-27 Black Bend

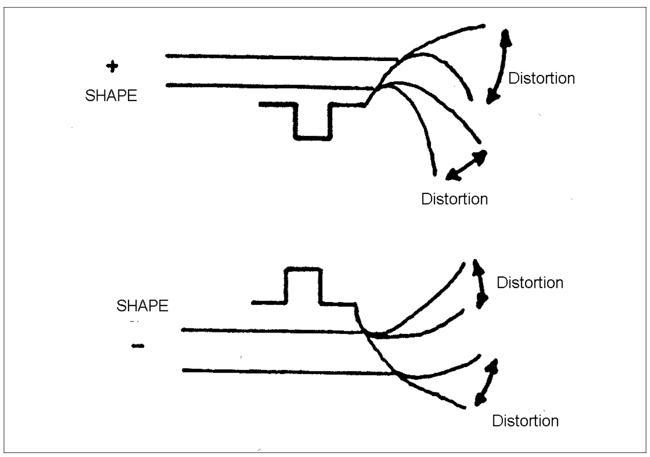


Figure 2-28 'S' Distortion

Two basic types of correction law are available, used separately or together : BLACK BEND (Figure 2-27) and 'S' DISTORTION (Figure 2-28).

V3, 4, 5 and 6 form a White Crush circuit, the onset of which is adjustable by R15 and the slope by R10 (see Figures 2-29 and 2-30).

This is called Black Bend, because the black part of the picture is emphasised relative to white and therefore when applied to the elastic delay line correction terminal, will produce a larger change of subcarrier phase at black than at white.

A1 is a double balanced modulator used as a multiplier where two inputs are video (one fixed, one variable) and another input from a DC bias control. Video from the emitters of V4 and 5 is applied to the base of V34 which is an emitter follower, the output is taken from the junction of R78 and 79. The signal at this point has its black level at -6V; this is applied to the -ve input on pin 4. In order to compensate for the Vbe of V34 and changes in the -12V power supply unit, a similar emitter follower is connected to the corresponding +ve input of the multiplier at Pin 1. Unlevelled shifted video is applied via R108 to the upper -ve input at Pin 10 and a variable bias to the corresponding +ve in-

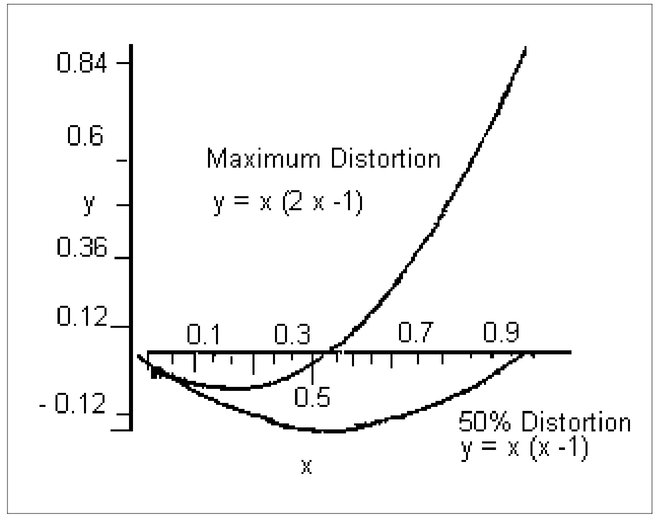


Figure 2-29 Effect of adjusting Slope Control (Distortion Fixed 50%)

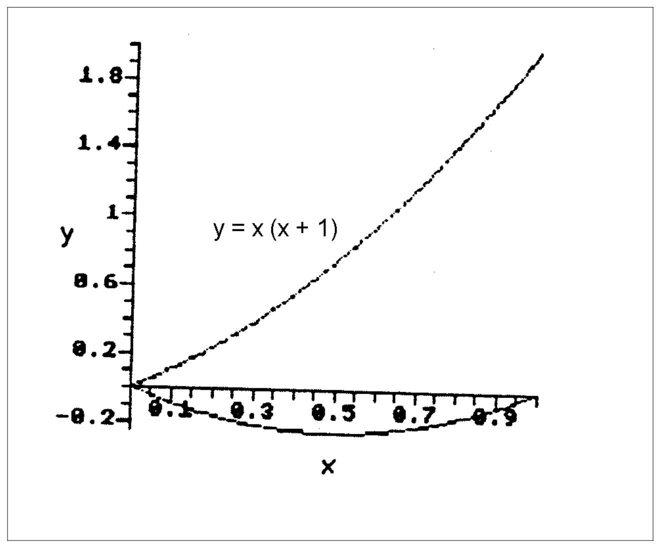


Figure 2-30 Effect of Adjusting Slope Control (Distortion Fixed 50%)

put at Pin 8 which may be either +ve or -ve depending on the setting of R110.

A balanced correcting signal is produced at pins 12 and 6. The black level voltage can be changed using the SENSE link to optimise the correction capabilities of the module for clockwise or anti-clockwise rotation of the subcarrier vector relative to the phase at white. The function of the multiplier is to produce a square law type of video distortion where the rate of change of slope and polarity can be adjusted together with a constant bias (+ or -). The shapes of distortions are shown in Figures 2-29 and 2-30, together with the transfer functions.

Either polarity of the above correcting signals is available by changing the SENSE links.

R92 controls the amplitude of correction. Control can be +ve or -ve, as previously stated. Any residual subcarrier is removed by notch components L15, C30 and 31. V38 is an emitter follower, which buffers the correction input of the

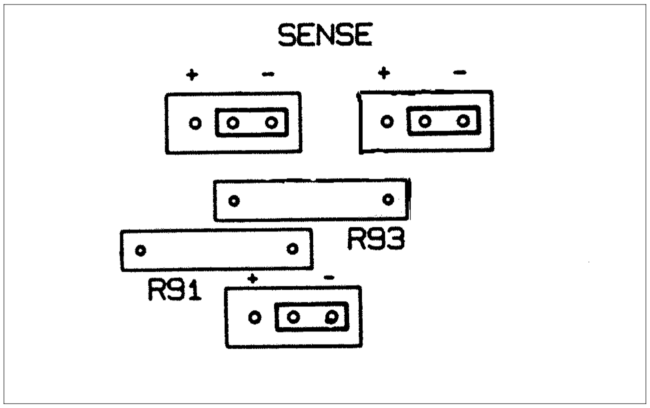


Figure 2-31 SENSE link settings

delay line.

The balance of the delay line may be trimmed by R31 and R70 to produce a good frequency response and to cancel breakthrough of the correction signal on to the video output.

The balanced video at the output of the delay line is amplified and unbalanced by the operational amplifier formed by V30, 31, 32 and 33 providing an output of 2 - 3V peak white, where black is at zero.

The output delay line is adjustable from 160 to 315ns. This is provided to enable the output video and carrier phase modulation to be correctly timed. If the timing is not correct a tilt will be noted across the double sideband portion of the transmitter swept response.

2.6.4 Carrier Phase Modulation

The video processing circuits are similar to the differential phase ones, allowing the same types of distortion signal to be generated, the only difference being that both +ve and -ve swings are available by turning R60 (± AMP) anti-clockwise or clockwise from its mid (off) position.

The carrier phase shifter circuit is driven by a CW IF signal so that at the module output phase modulation only is present.

V39, T1, R97 and C32 form the phase-shifting network, where the carrier input is provided by V40. V39 is a varicap diode across which the phase-shifting signal is applied via L16. Capacitance variations created by the phase shift signal cause the carrier signal from V40 collector to take a different path, either direct, or via T1, depending on the amplitude of correction required. R97 (SOT) ensures that very little AM is produced by this action. A3 and V41 both amplify and buffer the signal produced at the phase shifter output. R101 sets the output level, which is 1mW CW.

2.6.5 Test Procedure

a. Set R92 to its off position (anti-clockwise), and R115 fully clockwise.

Note:
In some early models it is clockwise.

b. Set the video delay line so that all sections are in except 40ns.
c. Set R31 and R70 to mid positions.
d. Connect a 1V 5-step staircase waveform to the video input.
e. Switch on and observe the video output on an oscilloscope terminated 75 ohms. Check that the signal amplitude is greater than 1V peak sync to peak white.
f. Connect SENSE links as shown in Figure 2-31 (for klystron operation).
g. Connect a sideband analyser to the video input and output. Sweep from 0 to 10MHz.
h. Turn R92 anti-clockwise then adjust R31 and R70 for best black white frequency response. Response should be within ±0.25dB to 5MHz with correction on and ±0.25dB to 5.5MHz with correction off.

Note:
In some early models R92 is turned clockwise.

i. Connect the staircase again and connect a vectorscope to the output.
j. Check that a rotation of the subcarrier vector (4.43MHz) of greater than 45° from black to white can be obtained. Under these conditions check that the linearity and differential gain are less than 5%.
k. For klystron operation connect link VIDEO SELECT to position DIRECT.
l. Connect a demodulator capable of measuring carrier phase to the IF output and a source of IF CW at a level of 1mW to the IF input.
m. Check that a resistor of around 50 ohms has been fitted for R97.
n. Using the demodulator, check that carrier phase modulation can be produced as R60 is rotated. When phase modulation is on look at the in-phase output from the demodulator and if necessary adjust the value of R97 to minimise the AM component. It should be possible for CPMs of 20° to reduce the AM to less than 5%.

Note:
As this is done it will be necessary to keep the output at 1mW using R101.

2.7 Aural and Visual Corrector

2.7.1 General Description

2.7.1.1 Aural Carrier Precorrection

Refer to the Aural and Visual Corrector block diagram given in Figure 2-32. The Aural IF carrier corrector consists of a phase modulator. The modulating signal used to drive the corrector is derived from the visual AGC detector. This provides a constant amplitude video signal which will be pre-distorted in a way which will aid the correction of the aural carrier.

The pre-distortion is created by the visual corrector stages in the process of ‘mopping up’ residual video distortions.

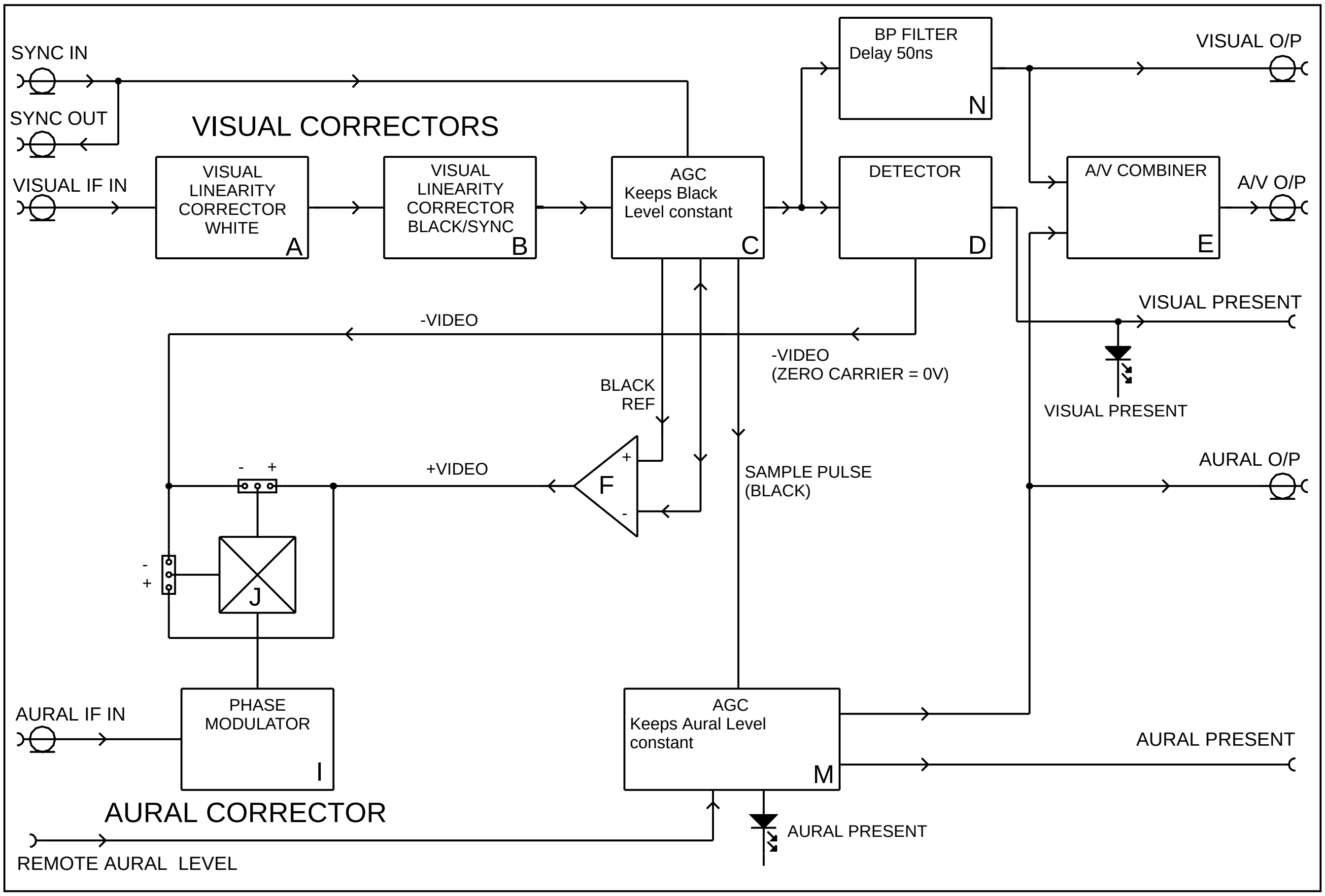


Figure 2-32 Aural and Visual Corrector Block Diagram

The detected video signal is fed via separate clipper circuits that allow optimum cancellation of the phase cross modulation.

Separate onset and slope controls are provided for the clippers and amplitude, distortion and shape for the analogue multipliers thereby enabling the shape of the video signal to be smoothly distorted at both black and white.

The amplitude modulator is a doubly balanced type. Very little phase modulation is produced in this circuit.

Aural AGC is incorporated which ensures that the aural power is held constant during adjustment of correction. The carrier level at a time corresponding to the visual back porch is used as the reference. Stability is further enhanced during adjustment by maintaining the video signal black level at zero volts.

A bandpass filter is incorporated in the visual signal after the detector and before the aural combiner. This makes up the delay of the detector and video circuits thus ensuring that the visual and aural compensating sidebands are in the correct phase.

2.7.1.2 Visual Correction

The visual correctors provide amplitude linearity correction prior to combining with the aural carrier. There are two correctors, one at white and one which operates in the mid grey to black region. Each have adjustable onset and slope controls.

2.7.2 Technical Data

2.7.2.1 General

Correct operation of the AGC is indicated by the dot being in the centre of the range.

Outputs (open drain) are provided to indicate the presence of the aural and visual signals, these are reflected by green LEDs on the module lid.

Correction on/off switches are provided for both the visual and aural corrections.

2.7.2.2 Visual

a. Visual IF Input:
   1. Level :
      1mW peak sync, 0.56mW black
   2. Impedance :
      50 ohms
b. Sync Pulse Loop Through Level :
   1V
c. Input Impedance :
   High

d. Visual Output :
   0.56mW black
e. Common Output :
   1mW peak instantaneous

2.7.2.3 Aural

a. Aural IF:
   1. Input Level :
      1mW CW
   2. Output Level :
      1mW linked to the Visual level when in AGC.

2.7.3 Technical Description

2.7.3.1 Visual Correctors

In each corrector there is one linear path and one correction path.

In the first correction stage (White End) (see circuit diagram 839 8121 833) the linear path is via C16 and V8.

The correction path is via R47, C36, A2, R18, V6 and then to the junction of R31 and 25 where the correction signal is summed with the linear signal.

Consider the simplified version of the correction circuit as detailed in Figure 2-34.

V1 is non-conducting for signals below Vref and hence its collector rises to the rail voltage of 12V. When the input signal exceeds Vref, V1 conducts and the amplitude of the signal excursion is determined (approximately) by the ratio Rc/2Re. The collector swing is the correction signal. It contains a video component and the second harmonic of the IF carrier frequency.

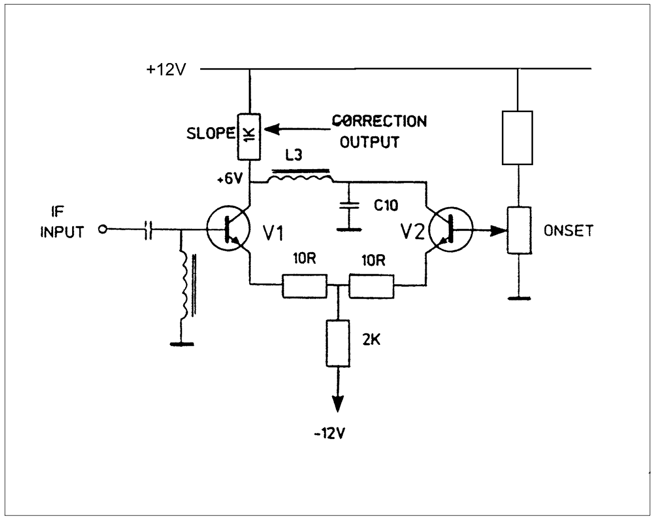


Figure 2-33 Video Component Cancellation

In the actual corrector circuit, the video component is cancelled by using a common collector load as in Figure 2-33.

R16 and C25 ensure that the wanted IF signal is not attenuated by this cancellation. The maximum slope of the correction (the amplitude of the correction added to the linear signal) is determined by the ratio of the load resistor to the emitter resistor. A potentiometer has been used for the load resistor so that the slope can be adjusted to suit transmitter requirements.

When the correction is combined with the linear signal (junction R31 and R25) the waveform shapes are as in Figure 2-35.

Note

The slope control can be set to zero so that the stage is linear only, as can the onset, if set to its maximum voltage (fully anti-clockwise).

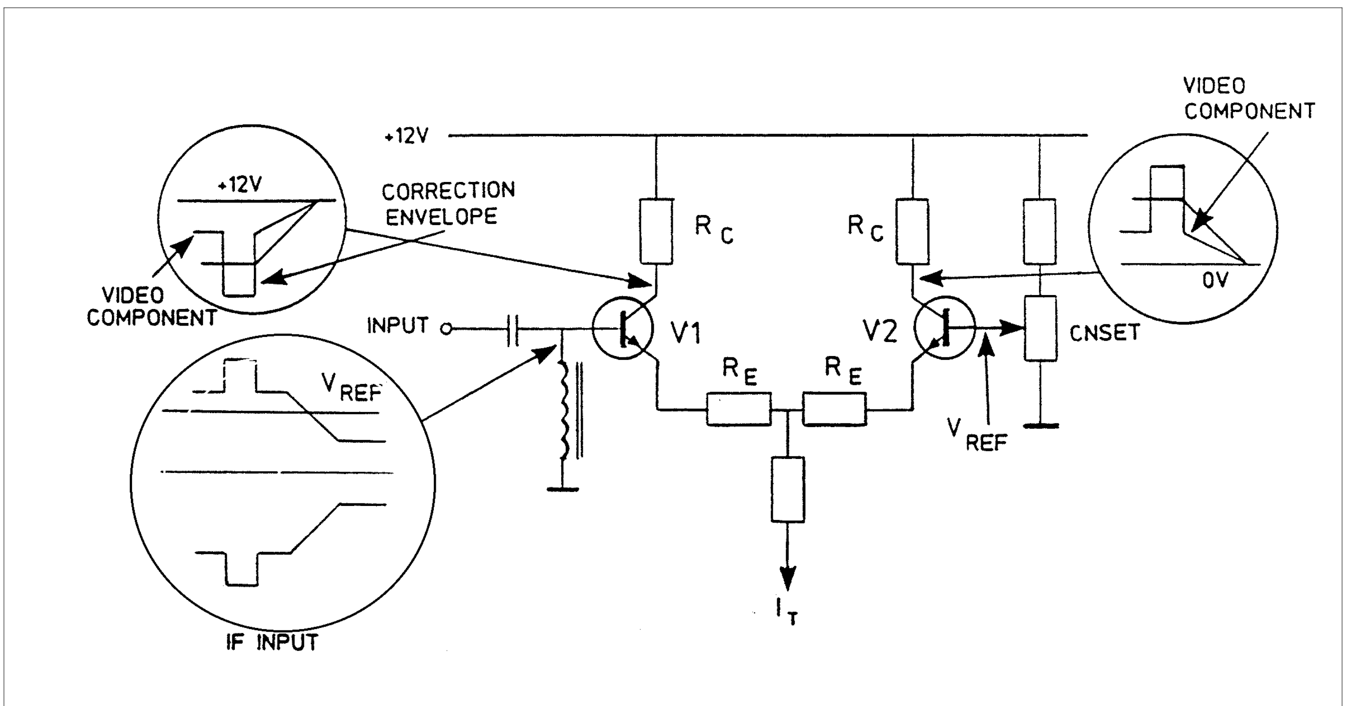


Figure 2-34 Simplified Version of Correction Circuit

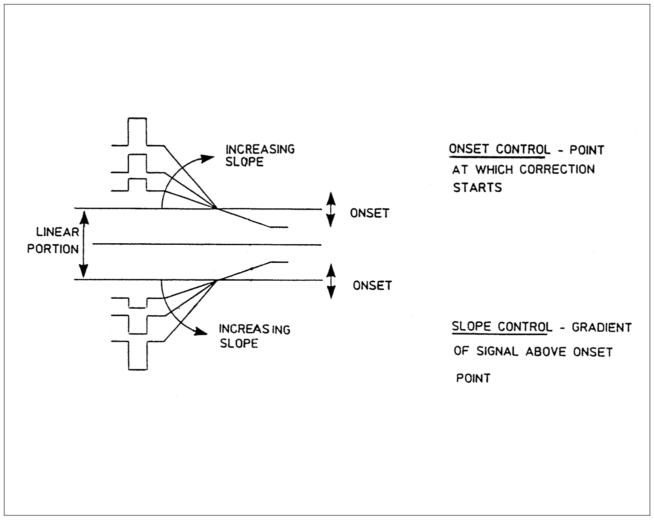


Figure 2-35 Mid-grey Corrector Waveforms

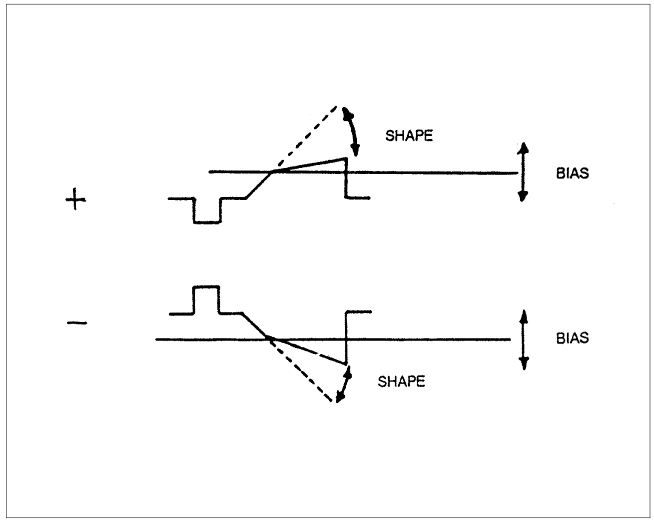


Figure 2- 36 Effect of A18

2.7.4 Input/Output Circuitry

Buffer amplifier V11, V4, at the input to the corrector stages, has a fixed gain. V25 is a mute switch.

Following the correctors is an AGC amplifier and a detector, A4 and its associated components form a video detector which produces a balanced output.

By using matched transistors as a differential pair, any offset effects are cancelled. The balanced video is converted to an unbalanced signal in A14 where zero carrier is at 0V, and black level is positive going. A11A provides buffering and gain and A11B inversion.

2.7.5 AGC Section

The input can be either:

1. - a sync pulse coinciding in time with the sync pulse of the incoming video IF input. In this case LINK 5 should be set in position ‘b-a’.
2. - or a sampling pulse adjusted for back-porch sampling. In this case LINK 5 should be set in position ‘b-c’.

In the first case, the timing section is used for generating the sampling pulse. A5 and A6 are dual monostables which are used to set the width of the pulse and where it appears.

A potentiometer R87 allows the adjustment of the 62µs inhibition period.

2.7.6 AGC Displays

If fitted, AGC metering is provided by a moving dot display consisting of A17. A similar display, A16 is provided for Aural AGC

2.7.7 Filter Printed Circuit Board

The Filter printed circuit board provides about 50ns delay, to ensure that the modulation on both the Aural and Visual IF carriers at the module output are coincident in time.

2.7.8 Aural Carrier Phase Modulation

A18 is an Analogue Multiplier where two inputs are video and another, input from a DC bias control. Positive and negative video from the detector is applied to links 3 and 4.

Positive or negative video may be multiplied by a positive or negative video signal with a variable bias so that both polarities and shapes of correction are available.

A7A buffers the correction signal and C97 with L20 form a subcarrier trap. The correction signal is available at TP8.

The carrier phase shifter circuit is driven by the Aural IF signal.

V1, L2, R5 and C4 form the phase-shifting network, where the carrier input is provided by V2. V1 is a varicap diode across which the phase-shifting signal is applied via L1. Capacitance variations created by the phase shift signal cause the carrier signal from V2 collector to take a different path, either direct, or via L2, depending on the amplitude of correction required. R5 (SOT) ensures that very little AM is produced by this action. A1 and V3 both amplify and buffer the signal produced at the phase shifter output.

2.7.9 Bench Setting Up Procedure

2.7.9.1 Visual Stages

a. Turn all potentiometers fully anti-clockwise except R215, R216, R217 (white adjustment potentiometers) which should be set at half position.
b. Connect a 1mW peak sync visual IF signal (to X1) and a source of sync pulses which are correctly timed (to X6).
c. With the VISUAL CORRECTION (S1) turned OFF and the AGC (LINK 1) set to MANUAL, check that at least 0.75mW black level is available at X4 when R54 is fully clockwise. If this black level cannot be achieved, adjust R217 to increase the gain (clockwise = more gain).
d. Set the level to 0.56mW black level using R54 (VIS MIN GAIN). Adjust C113 to minimise the residual IF present on the video at A14 pin 6. Disconnect the

visual IF input (X1). Then adjust R215 to obtain 0V at TP3.

e. Adjust R87 to set up the monostable pulses. Check that they are as follows:
   1. TP9 62µs ± 1µs (INHIBIT NON RETRIG).
   2. TP6 0.5µs ± 10% (SAMPLE PULSE DELAY) .
   3. TP5 1.7µs ± 10% (SAMPLE PULSE INHIBIT).
   4. TP7 3µs ± 10% (SAMPLE PULSE LENGTH).

f. Change LINK 1 to the AGC position and adjust R118 (VISUAL POWER) to obtain 0.56mW black level at the visual output X4. Check that the VISUAL AGC LED bar graph indicator (A17) is not at one end of its range. Check that the VISUAL PWR LED (H2) is illuminated.

g. Switch the correction (S1) ON and check the operation of each stage by observing a waveform monitor connected to a demodulator at the visual output (X4). The white corrector should provide at least ±5% differential gain correction at white relative to mid grey (adjustments are provided by R18, SLOPE and R41, ONSET). The mid grey corrector should provide at least 20% stretch at black relative to white (adjustments are provided by R17, SLOPE and R35, ONSET).

h. Check Visual response using a sideband adaptor with a wideband modulator. The response should be within 0.5dB from 41.25 to 47MHz.

2.7.10 Aural Stages

a. Apply a CW signal at 41.25MHz to the aural input (X2). Set LINK 2 (AGC/MAN) to MANUAL and check that at least 1.5mW is available at the aural output (X8) When R154 (AURAL MANUAL) is fully clockwise. It may be necessary to adjust R4 (AURAL GAIN) to achieve this.

b. Connect an oscilloscope to TP11 (LEVEL). Remove the aural IF input (X2) and adjust R216 to obtain 0V at TP11. Reconnect X2 and adjust R154 to obtain 1mW at the aural output (X8). Adjust R137 so that the detected voltage is 2.5V ±0.1V. Check that the AURAL PWR LED (H3) is illuminated.

c. Set LINK 2 to AGC and check that 1mW is available by adjusting R151 (SET AUTO AURAL LEVEL). Note that there must be a Visual signal present for this test. Check that the AURAL AGC bar graph may be centred by adjusting R4. Remove the Visual input and check that the Aural signal drops by at least 10dB and that the AURAL POWER LED is ***not*** illuminated.

d. With the Visual signal present, observe the combined output (X9). Adjust R151 (SET AURAL LEVEL) so that the visual to aural ratio is 10dB. It may be necessary to adjust R161 (AOT resistor) to achieve this.

Note

In the following procedure (e) check that the relevant controls are operating correctly. Adjustment of these controls would normally be made when setting up the transmitter. LINK 3 and LINK 4 should be linked appropriately to connect positive and negative video.

e. To check the phase modulation, off-tune the spectrum analyser so that it slope-detects (converts phase modulation to amplitude) on the side of the bandwidth limiting filter. Check that a video signal appears as the phase modulation controls are adjusted (R208, PHASE MOD LEVEL; R209, PHASE MOD SHAPE; R20, BIAS - operates in conjunction with R209 to change the shape) and that if the analyser is tuned back to the peak, that the modulation disappears.

f. When check (e) has been satisfactorily completed, turn the controls to the ‘OFF’ position ready for system setting up.

2.8 Aural Corrector Assembly

2.8.1 General Description

This unit accepts separate visual and aural IF inputs and provides a combined IF output with aural precorrection. The aural AGC keeps the visual to aural ratio constant regardless of the level of correction or level of temperature changes.

To achieve aural pre-correction the aural signal is combined with a sample of the vision signal and applied simultaneously to two identical non-linear circuits. The outputs of these two non-linear circuits are summed to give the precorrected aural signal. Because of the phase relationship between the two non-linear paths, the vision sample signal is cancelled and only the aural signal remains. The resulting signal carries inter-modulation products that are opposite to those generated in the power amplifier.

2.8.2 Technical Data

2.8.2.1 General

a. Links and Switches:

LK6 :	Aural Level Manual/Auto
LK1 and LK3 :	Stage 1 Expand/Compress
LK2 and LK4 :	Stage 2 Expand/Compress
S1 :	Correction ON/OFF

b. Potentiometers:

R167 :	Aural Level in AGC Mode
R166 :	Aural Level in Manual Mode
R115 :	Combined Output Level

2.8.2.2 Visual

a. Visual IF Input Level : 1mW peak sync
b. Sync Pulse Loop Through : 1V positive

2.8.2.3 Aural

a. Aural IF level : 1mW

2.8.2.4 Power Requirements

a. +12V : 700mA
b. -12V : 80mA

2.8.3 Technical Description

Refer to schematic 839 8121 919 Sheets 1 and 2.

The Vision IF is connected to X11. After amplification by A9 it is split into two paths in A27. One is the main vision path, the other is the correction path. In the correction path the signal is filtered by the Chrominance Reject Filter PCB and applied to the transformer T2. T2 produces two signals 180 degrees out of phase which are applied simultaneously to combiners A25 and A26. The Aural IF is applied to X6, and then applied simultaneously to combiners A25 and A26.

A25 and A26 produce a combined vision and aural signal. These two combined signal are applied to two identical linearity correctors (sheet 2 of schematic). Only the first corrector is described here. This corrector consists of the components connected between splitter A32 and combiner A33. After splitting, the signal is fed through three parallel paths.

The first path consists of V1/V2 (PIN diode attenuator), amplifier A5, limiter A35 and associated components, V3/V4 (PIN diode attenuator), transformer T1 and amplifier A39. A35 and associated components form a non-linear circuit which expands the signal at high level (‘Black Expand’). PIN diode attenuator V1/V2 is voltage controlled and determines the onset of the correction. Pin diode attenuator V3/V4 is also voltage controlled and determines the slope of the correction.

The second path is very similar to the first one. It consists of V5/V6 (PIN diode attenuator), amplifier A6, limiter A36, V7/V8 (PIN diode attenuator), and delay filter C34, L10, C35, L11, C36. The main difference from the first path is that the limiter A36 is configured to crush the signal at high level (‘Black Crush’).

The third path consists of a resistive pad, a delay filter C37 L12, C38, L13, C39 and another resistive pad. This path is the main linear path.

The correction signal from the first and second path recombine with the linear signal in combiner A33. Links LK1 and LK2 allow a selection of the sign of the correction of each path (expand or crush).

The second corrector is in all aspects similar to the first one. It comprises the components between splitter A31 and combiner A30. Both correctors have adjustable onset and slope for each stage. Their controls are linked together so that they have the same correction curve. These controls are :

ONS1	ONSET OF STAGE 1	Potentiometer R57
SLO1	SLOPE OF STAGE 1	Potentiometer R59
ONS2	ONSET OF STAGE 2	Potentiometer R58
SLO2	SLOPE OF STAGE 2	Potentiometer R60

The two signals produced by the two correctors recombine in A34. Because of the phase relationship between these two signals, the vision part of the signal cancels in A34 and only the aural and the third order inter-modulation product remain. Therefore the output of A34 is essentially a corrected aural signal. Variable capacitor C43 and potentiometer R55 are set so as to equalise the delay in the two correctors and to obtain good cancellation of the vision in A34.

The corrected aural signal is applied to amplifier A16 (schematic sheet 1) and A17, and is filtered by the IP Reject Filter PCB to further reduce the level of vision IPs present. The signal goes through V15/ V16, PIN diode attenuator, which controls the level, is amplified by A18 and then is combined with the Vision IF in combiner A24. R115 allows adjustment of the combined IF level. After further amplification in A19, the combined signal, Vision plus Corrected Aural IF, is output to X1.

A sample of the corrected aural signal is made available at X2 via buffer V26, for set-up and monitoring purpose.

A sample of the corrected aural signal is applied to the level detector A23 and associated components. Potentiometer R164 determines the gain of this detector. After buffer A22 the detected aural signal is sampled by FET V14 during the back-porch period of the Vision IF. The loop amplifier A14B compares the value of the aural signal to the voltage from potentiometer R167 (‘AUTO AURAL’). If link LK6 is in the AUTO position then A14B controls the PIN diode attenuator V15/V16. The back-porch level of the aural signal is therefore held constant. If link LK6 is in the MAN position then the level of the aural signal is manually adjusted by potentiometer R166.

The sampling pulse for FET V14 is elaborated from the Sync pulse input on X7 by the buffer inverter V9/V10 and the timing section A12/A13.

2.8.4 Setting-up Procedure

2.8.4.1 Initial Settings

a. Potentiometer R164 (DETECTOR GAIN) fully clockwise.
b. All other potentiometers fully anticlockwise.
c. Switch S1 to OFF.
d. Link LK6 to MAN.
e. Links LK1, LK2, LK3, LK4 to bottom position.

2.8.4.2 Plug-in Filter Boards

During the following procedure refer to the frequency response curves of the filter boards for the chrominance reject filter (Figure 2-37) and the IP reject filter (Figure 2-38).

2.8.4.3 Visual Level

a. Apply a 1mW peak sync visual IF signal to X11.
b. Adjust R115 to obtain a 0.5mW peak sync signal at X1.

2.8.4.4 Aural Circuit

a. Keep a visual IF signal connected to X11.
b. Apply a 1mW aural IF signal to X7.
c. Connect a spectrum analyser to X1 (Combined Output).
d. Adjust R166 (AURAL MAN GAIN) so that the visual to aural ratio is 10dB.
e. Connect the spectrum analyser to X2 (Aural Monitoring Output).

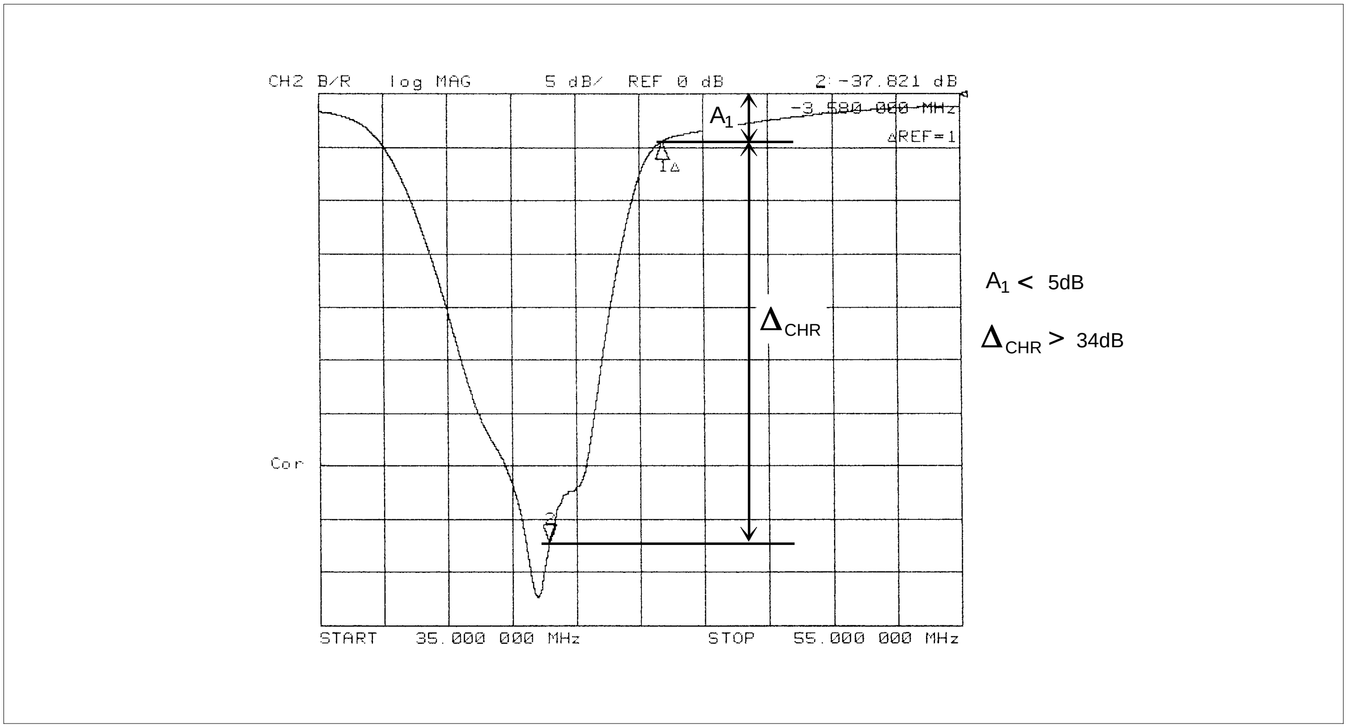


Figure 2.37 Chrominance Reject Filter

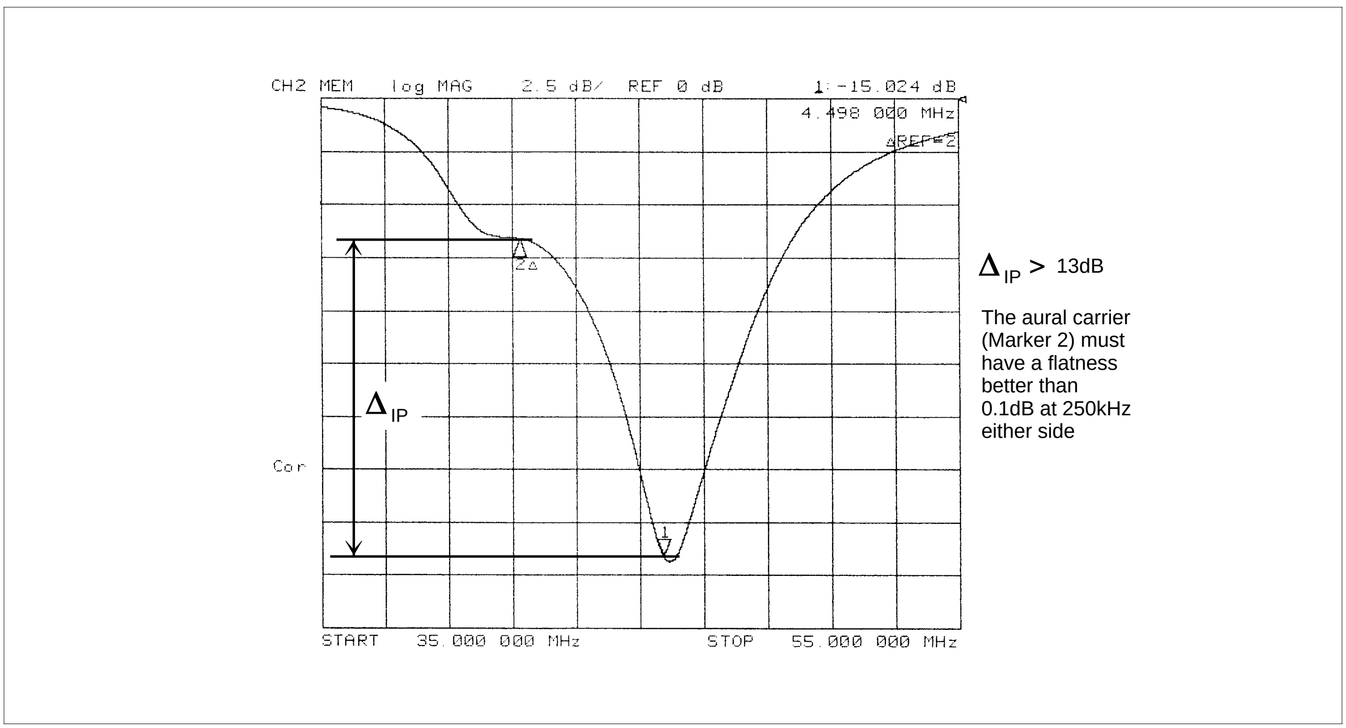


Figure 2-38 IP Reject Filter

f. Adjust trimmer capacitor C43 and potentiometer R55 so that the tone at the vision frequency is minimised.

g. This tone should be at least 15dB below the aural carrier.

h. Re-connect the spectrum analyser to X1 and, if necessary, re-adjust the visual to aural ratio to 10dB.

2.8.4.5 Frequency Response

Check the frequency response using a spectrum analyser and a side-band adapter.

a. Turn potentiometer R254 (FREQUENCY RESPONSE) clockwise to compensate for a tilt in the frequency response at the combined IF output X1.

b. Re-adjust the output level potentiometer R115 (O/P LEVEL) (0.5mW black, vision only) and the vision to aural ratio with R167 (AUTO AURAL).

2.8.4.6 AGC

a. Connect a positive going sync pulse to X7.

b. Adjust R94 to obtain a 60µs pulse at TP1.

c. Check the following timings and change the corresponding AOT resistor if needed. These pulses are positive going.

TP3	1.7µs ±10%	R96
TP2	0.5µs ±10%	R177
TP4	3µs ±10%	R95

d. Change LK6 position to AUTO.

e. With the spectrum analyser connected to X1, adjust potentiometer R167 so that the visual to aural ratio is 10dB.

2.8.4.7 Correction

a. Set correction 'on' with S1.

b. Connect a video IF signal modulated with a ramp or staircase to X11.

c. Adjust R57, R58, R59, R60 and check that it is possible to change the shape of the envelope of the aural carrier.

2.9 Group Delay Correction Assembly

2.9.1 General Description

The unit contains six active all-pass phase equaliser sections each of which is identical except for the value of the phase adjusting resistor and the tuned circuit resonant frequency. These two items are selected at the time of test and are determined by the shape of the group delay curve to be corrected.

The overall gain of the unit is unity and the input signal level is 1mW peak sync.

This unit incorporates a light-emitting diode to monitor the visual IF output.

2.9.2 Technical Data

a. Input Impedance : 50 ohms. TNC connector.

b. Input VSWR : 1.5 maximum.

c. Input Level : Up to 1mW peak sync.

d. Gain : 0dB ±0.5dB (averaged over the frequency range 32-41MHz).

e. Amplitude/Frequency Response:
Flat within ±0.2dB over the frequency range 33-41MHz.

f. Group Delay Correction : Adjusted to meet system requirement.

g. Low-frequency Linearity : Better than 1%.

h. Differential Gain : Better than 1%.

i. Differential Phase : Better than 1°.

j. Output Impedance : 50 ohms. TNC connector.

k. Output VSWR : 1.2 maximum.

l. DC Power Requirements :
+12 Volts at 260mA.
-12 Volts at 210mA.

m. Dimensions:
Width : 37mm
Depth : 310mm
Height : 140mm

n. Weight : 624g approximately.

2.9.3 Technical Description

2.9.3.1 The Basic Equaliser Circuit

The principles of operation of the basic equaliser circuit are best understood by referring to Figures 2-39 and 2-40.

In Figure 2-39 (a) the amplitude, phase and group delay characteristics of parallel resonance are illustrated, together with the vector diagram of the voltage across the circuit (er) relative to the current through it (im), when the frequency is varied from zero, through resonance (wo) to infinity.

The diagrams in Figure 2-39 (b) illustrate the characteristics and vector diagram which result from the vector sum of e'r and another voltage e of the same frequency. The phase of e is constant and is in opposition to er when the tuned circuit is resonant. It can be seen that as e is increased from zero, the centre of the circular locus of the vector sum er is moved in the direction of e by an amount equal to the magnitude of e. As it does so, the slope of the resultant phase angle increases, and the magnitude and shape of the amplitude characteristic changes in accordance with the illustrated family of curves.

> When: e = er max/2
> e'r = e and is constant at all frequencies. The amplitude of the resultant output signal is therefore constant and only the phase and hence the group delay characteristics are frequency dependent.

Another significant feature of this circuit is that the maximum possible phase displacement of vector e'r is ±180° whilst that of er is ±90° only.

The circuits used here are all adjusted so that e = er max/2.

Therefore, by choice of the Q of the tuned circuit and by cascading a number of circuits, any practical degree of group delay equalisation can be achieved.

If the vectors e and er are not in precise phase opposition when the tuned circuit is resonant then the centre of the locus of er is displaced as illustrated in Figure 2-40. The amplitude response of the circuit is also changed as illustrated.

2.9.3.2 Group Delay Corrector PCB

Refer to Circuit Diagram 3913 466 24830 (Sh. 130-1).

The first section only will be described as the other five are similar.

The input is terminated by a combination of R4, R2, R1 and R8 and passes to the summing output amplifier V2 and V3 via the phase shifting network R1, R8, C6 and C7.

Table 2-5 Alignment Details - Frequency

Section Number	Frequency (MHz) System G G/D2	System M G/D2	System I G/D2
1	34.1	42.0	34.4
2	35.4	42.25	35.1
3	36.7	43.7	36.9
4	37.9	44.7	38.7
5	38.7	45.4	39.9

Table 2-6 Alignment Details - Controls

Section No.	***Connect Input between tags***	Amplitude Control	Phase Control	***Frequency Control***	***Q Control***
1	Input socket X1	R2	C6	L1	R7
2	B-C	R17	42.25	L4	R22
3	E_F	R32	C30	L7	R37
4	H-I	R47	C42	L10	R52
5	K-L	R62	C54	L13	R67
6	N-O	R77	C66	L16	R82

After passing through a phase-inverting transformer T1, the input signal is also applied to the emitter of V1, a common-base amplifier. The voltage gain of this stage is determined by the ratio of R6 in series with R7 and R4 in series with R2. Thus R2 becomes a gain control for the stage and hence controls the amplitude of the resonant signal at the base of the summing amplifier V2.

Since the input impedance of the amplifier V2 and V3 is very low, due to feedback, the Q of the resonant circuit L1 and C4 is determined principally by R6 and R7. Adjusting the values of R6 and R7 therefore, changes the shape and magnitude of the group delay correction curve and are selected when the unit is tested.

The summing amplifier V2 and V3 is a wide-band DC-coupled feedback amplifier having a low output impedance. The feedback resistor R11 is adjusted to make the overall gain of the section unity. A low-pass filter L2 and C10 restricts the bandwidth of the section to approximately 70MHz.

2.9.4 IF Monitoring

IF output at V18 emitter is detected by V19, V20. The rectified outputs cuts off V21; V21 collector rises, switching on V22. V22 conducts and lights led H11, which is mounted on the front panel.

2.9.5 Setting-up Procedure

The following setting-up procedure is applicable to new untested units or units which have been repaired following their failure in service. After completing the procedure the unit should be re-installed into the system and final adjustments carried out to meet the overall system requirements.

Note:

The setting-up is performed section-by-section from output back to input.

a. Connect a display unit to the output socket X4 via a 50 ohm detector. Remove link ‘m-n’ on section 6 and connect a sweep generator to the test points ‘n-o’ via a 50 ohm coaxial cable.
b. Turn amplitude control R77 fully clockwise and Q control R82 to approximately mid position.
c. Adjust L16 to produce a dip in the response at the frequency indicated in Table 2-5.
d. Adjust the amplitude R77 and phase C66 controls to produce a flat amplitude response from 35MHz to 55MHz.
e. Remove the coaxial cable and reconnect link m-n.
f. Repeat the above procedure for the remaining sections in reverse numerical order, using Tables 2-5 and 2-6, progressively adding sections until all have been aligned. It may be necessary to slightly readjust some of the amplitude and phase controls to obtain a flat amplitude response for the whole unit ±0.4dB.
g. Using a sideband response analyser, display the wideband group delay characteristic. Adjust the Q controls (slight adjustment of frequency control if necessary) of each stage to optimise the result, which should be within ±20ns across the vision passband.

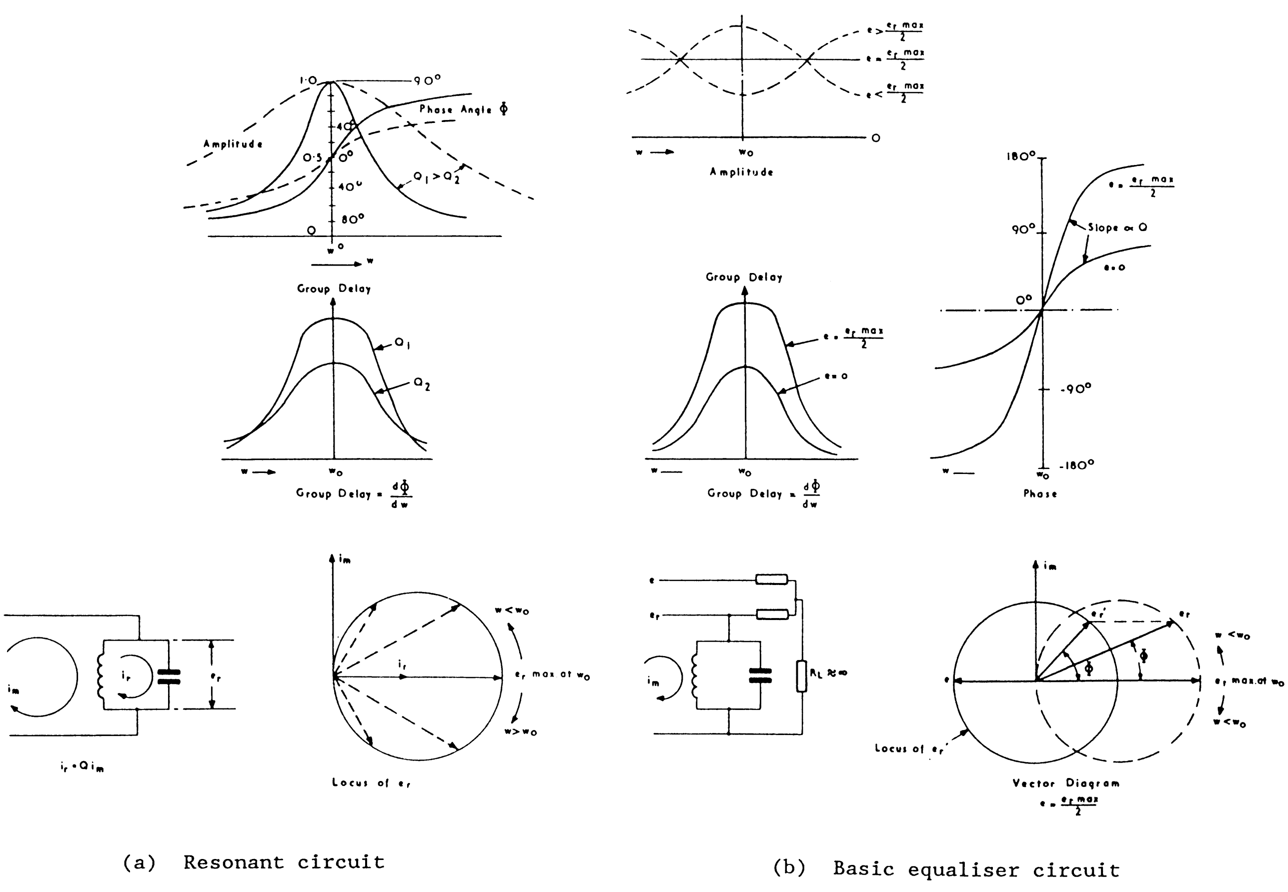
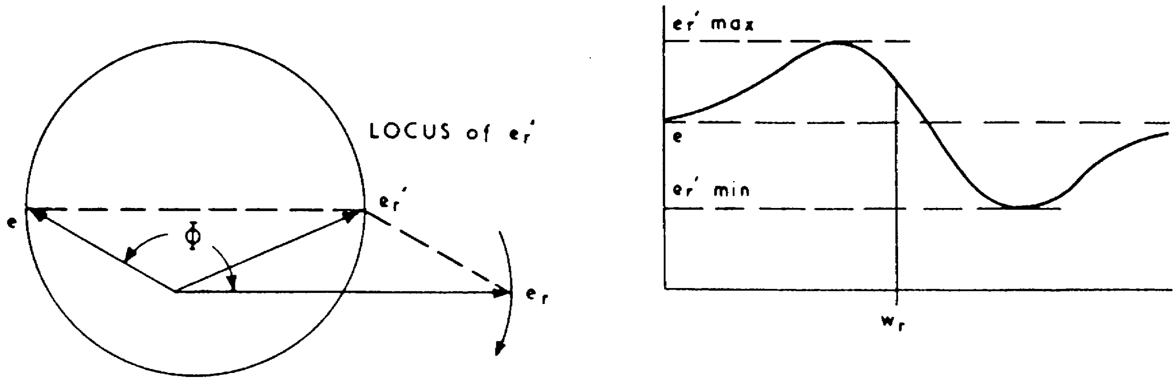
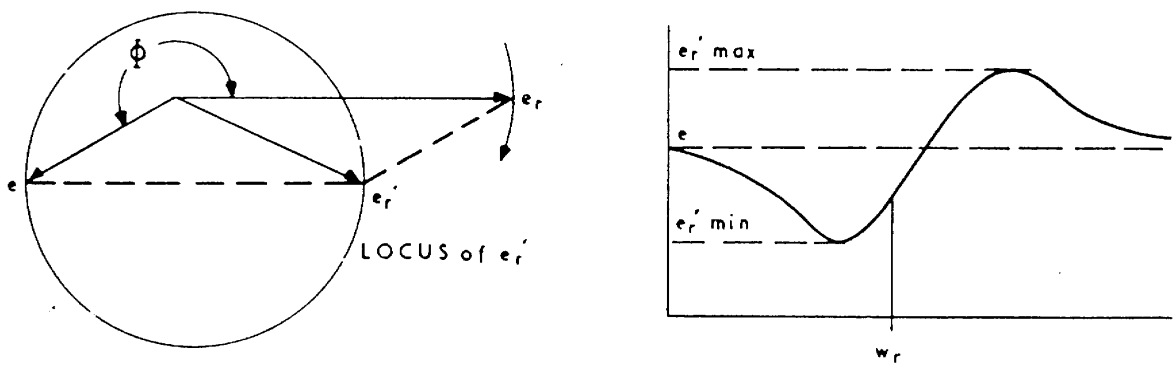


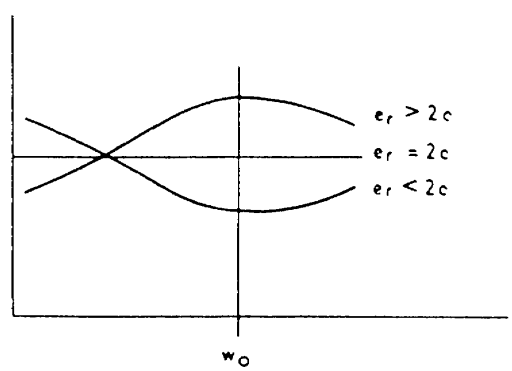
Figure 2-39 Basic Equaliser - Universal Characteristics



(a) Vectors & Characteristic for $\Phi < 180°$



(b) Vectors & Characteristic for $\Phi > 180°$



(c) Characteristic for $\Phi = 180°$

Figure 2-40 Basic Equaliser - Test Displays

h. Display the vision amplitude response again and adjust the Amplitude and phase control if necessary to obtain a flat response ±0.4dB.

Note:

Some iteration between steps (g) and (h) may be necessary in order to meet group delay and amplitude response specifications.

i. Check that the gain throughout the unit is unity. R11, R26, R41, R56, R71 and R86 may be adjusted, within the range 390 to 470 ohms, to achieve this.

j. Final adjustment of this module should be carried out in the transmitter into which it is fitted, but an approximate alignment may be achieved by referring to Table 2-6.

2.10 Combined Mixer/Up-converter Assembly

2.10.1 General Description

The Combined Mixer/Up-converter assembly uses one circuit for combined aural and vision signals.

The local oscillator signal is mixed with the modulated aural and visual IF signal and amplified before being fed to the next stage of the mixer assembly.

An IF monitor output is provided (if required) for the purpose of ALC of the mixer input.

2.10.2 Technical Data

2.10.2.1 Return Losses

a. LO Inputs (X3),510 to 900MHz :
Equal to or better than 15dB.

b. IF Inputs (X4),DC to 100MHz :
Equal to or better than 20dB. (To measure the IF return loss, a LO signal must be present.)

c. RF outputs (X2), 470 to 860MHz :
Equal to or better than 20dB.

d. IF outputs (X1),20 to 100MHz :
Equal to or better than 20dB.

2.10.2.2 Levels - Visual and Aural

a. LO Input Level (X3) : 5mW±2dB
b. IF Input Level (X4) : 1.0mW PIP
c. RF Output Level (X2) : 0.1mW PIP
d. IF Output Level (X1) : 0.1mW PIP
e. Differential Gain (RF O/P) : < 2 %
f. LF Non-linearity (RF O/P) : < 2 %
g. IPs (measured at channel filter output):
< 60dB
h. 12V Supply Current : 350mA

2.10.3 Technical Description

A1 is a double balanced surface mounted mixer, the IF input being supplied via a 6dB pad formed by R1, R2, R16 and R31. This improves the return loss at X4 and enables a standard level of 1mW PIP (peak instantaneous power) to be used.

The Local Oscillator for the mixer is supplied from a saturating amplifier formed by V1 with resistors R22, R21 and R35 providing a 50 ohm source. The saturated power available at the mixer input is 7.5dBm. V3 makes up the loss generated by the 6dB pad at X3. The 6dB pad (R3, 4 and 5) and V3 buffer the mixer and saturating amplifier providing a good input return loss at X3.

V2 at the mixer RF output is a low noise amplifier (no series or shunt feedback is used as this degrades the noise figure of the transistor). C15 and the 6dB pad formed by R10, 11 and 25 provide slope correction across the UHF band for the mixer and low noise amplifier combination. V5 provides further gain so that the conversion loss of the module (IF to required UHF output) is about 6dB.

An IF monitor output at X1 is provided for the purpose of ALC of the mixer input (modulation assembly output). V4 is an emitter follower which buffers the IF at X4. R5 ensures that X1 has a good return loss and an output level similar to that at X2.

2.10.4 Test Procedure

2.10.4.1 Aural and Visual

a. Measure the current drawn from the +12V supply. This should be approximately 180mA.
   1. Measure the return loss of all ports:
   2. LO inputs should be better than 15dB, 470 to 900MHz.
   3. IF inputs should be better than 20dB, DC to 100MHz when a LO signal is present.
   4. IF output should be better than 20dB, 20 to 100MHz.
   5. RF output should be better than 20dB, 470 to 860MHz.

2.10.4.2 Visual Only Signal (to check operation)

a. Connect a source of local oscillator (signal generator) to the LO input (X3), and an IF source which can be vision modulated to X4. Set the LO level to 7dBm (5mW) and the IF to 0.58mW black level.

b. Check the level of the wanted tone (LSB) on a spectrum analyser when the IF input is at black level CW and as the LO is varied from 510 to 900 MHz. The level should be from 0.1 to 0.2mW (-10 to -7dBm).

c. Check the level of local oscillator breakthrough. This should be more than 20dB below the wanted signal (it may drop to 18dB at 860MHz when LO = 900MHz).

d. Check the IF level on X1. This should be 6 to 7dB lower than the IF input signal.

e. Using a suitable receiver and waveform monitor check the differential gain and LF non-linearity when a test signal modulated VSB filtered IF signal is applied to X4. These should be less than 2%.

f. Connect a combined Aural and Visual signal of 1mW PIP and check that the IPs are better than -60dB at the output of the channel filter (set up for the channel of operation).

2.11 IF and Master Oscillator Assemblies

2.11.1 General Information

The IF and Master Oscillators are essentially identical, differing only in frequency. Both use the same crystal oscillator assemblies detailed in section 2.11.4.

2.11.2 IF Oscillator

The IF Oscillator is identical, except in frequency, to the master oscillator and contains a third overtone crystal oscillator housed in a temperature controlled oven. By selection of the required crystal the oscillator is capable of producing frequencies in the range 37MHz to 66MHz.

Three signal outputs are provided, each set to a nominal 1mW into 50 ohms.

Fine frequency control is achieved by adjustment of the internal potentiometer or by applying an external control voltage.

IF NORMAL is indicated by a green LED.

2.11.3 Master Oscillator

The Master Oscillator (P) , is identical to the IF Oscillator except for the crystal frequency being selected for correct frequency multiplication to produce the local oscillator UHF frequency. Levels of 1mW CW are set at PX1, PX2, PX3.

2.11.4 Crystal Oscillator Assemblies - General Description

This unit contains a third-overtone crystal oscillator, capable of operation between 37MHz and 66MHz housed in a proportionally controlled oven. Three signal outputs are provided, each providing a level of 1mW into a 50 ohm load. The oven temperature is controlled by a thermistor and high-gain DC amplifier. The oscillator supply is regulated to reduce to a negligible level, frequency shifts due to supply voltage changes. Fine control of the oscillator frequency is obtained by adjustment of the voltage applied to a varactor diode, either from an internal potentiometer control accessible through the module cover, or from an external control voltage. In Version 40323 the fine control (EXT/INT) is selected by means of a switch on the outer case. For version 40324 selection is made by internal wire-link connections on the printed circuit board. Two 12V supplies are required to power the oscillator and oven separately so that the oven may be continuously powered, though a single supply will suffice for test purposes.

The presence of IF output is monitored by a green light-emitting diode on the module casing. Also, a logic signal is provided for external monitoring.

2.11.5 Technical Data

a. Frequency Range : 37 to 66MHz.

b. Crystal Type : 3rd overtone. Holder Type HC - 26/U.

c. RF Outputs :
3 x 50 ohm TNC sockets each giving approximately 1mW.

d. Frequency Stability : Long-term ±1.5 parts in 10^{-7}
Medium-term ±5 parts in 10^{-8}.

e. Power Requirements:
   1. Oven: 12V 1A*
      * A separate supply is preferred for the oven.
   2. Oscillator : 12V 70mA

f. Control Voltage Input Range (for use with frequency synthesiser in precision offset operation) :
+3V to +20V DC.

g. Ambient Temperature Range : -10°C to +45°C.

h. Dimensions (inclusive of screw heads, sockets and terminals) :
Width 162 mm
Depth 94 mm
Height 54 mm

i. Weight : 440g (approximately).

2.11.6 Technical Description

Refer to the circuit diagram, Sh. 130-1.

2.11.6.1 Oven Control Circuit

The oscillator circuit board is mounted in a small cast aluminium box which serves as an oven. The oven is heated to 75°C by two power transistors V9 and V10 bolted to opposite sides of the outer surface. A thermistor R25, positioned inside the oven wall, senses the oven temperature and is connected in a bridge circuit with R21, 23, 24 and R22. R22 is used to set the oven temperature to 75°C. R26 and R27 and Zener diode V7 reduce the effect of supply voltage changes on bridge balance by keeping the thermistor dissipation to a low and constant level. R21, R22, R23, R24 and V7 are mounted beneath the oven on the Oven Regulator and Output Amplifier board and are thus isolated to some extent from changes in ambient temperature. R22 is mounted close to the oven for the same reason. The outputs of the bridge will be balanced at 75°C and any departure from this temperature will produce a differential input to the integrated-circuit DC amplifier A2. This amplified change is fed via the emitter follower V8 to the parallel power transistors V9 and V10 whose collector dissipation is changed to compensate for the original change in oven temperature.

Two devices are used to distribute the heat more evenly and are screwed directly to the oven case. The collector current of V9 and V10 is set individually by adjusting the values of R29 and R30 respectively so that the maximum available current is 1A, giving a dissipation of 11W.

Dissipation at an ambient temperature of 25°C is approximately 2.5W. R28 sets the gain of A2 at a high value consistent with avoiding temperature “hunting”. R31 is in series with the oven supply so that the oven current may be ascertained using an external meter.

2.11.6.2 Oscillator Circuit and Output Stages

The oscillator transistor V1 which operates in the grounded-base mode has a collector circuit tuned by C1, C2, and L1. The value of C1 is set at the factory and depends on the frequency of operation. Positive feedback is taken from a tap on L1, via the series-resonant third-overtone crystal B1, to the emitter. C3, C4 and the varicap diode V2 are arranged in series with the crystal to provide a degree of frequency pulling to overcome crystal manufacturing tolerances and ageing. C3 gives a coarse frequency adjustment which will not normally require attention.

Fine frequency control is obtained by adjustment of the voltage on V2 by setting R19 (FINE FREQ), accessible through a hole in the outer case, or applying a voltage to the feed-through capacitor C20 (EXT FREQ CONTROL) mounted on the end of the case. The limits of this applied voltage must lie between +3V and +20V with respect to ground. The selection of internal or external fine frequency control is provided by a switch for version 40323, and by wire link connections for 40324. The output from the oscillator stage is taken from the same tap on L1 and passed to a buffer amplifier stage V3 and its associated components. One printed circuit board contains the oscillator and the buffer amplifier and is mounted in the oven. The output from the buffer amplifier is taken from the collector of V3 and fed simultaneously to three identical output stages, V4, V5 and V6 and their associated components. Each stage has a source impedance of 50 ohms provided by broad band transformers T1, T2, T3 and delivers a level of 1mW in 50 ohms to each of the three output sockets. These levels are adjusted by choosing the values of R14, R16 and R18. The supply to the oscillator, amplifier and output stages is +8V which is derived from an integrated circuit regulator A1 operating on the incoming +12V oscillator supply.

2.11.6.3 Crystal Frequency

For use as the intermediate frequency crystal oscillator the crystal fitted is a third-overtone crystal operating at the intermediate frequency.

For generation of the vision carrier frequency (fv) the crystal fitted is a third-overtone crystal operating at a frequency calculated from the following formula:

$$\text{f crystal} = \frac{fv + IF}{A}$$

where A is a constant for a range of vision frequencies, as follows :

a. VHF Band I : A = 2
b. VHF Band III : A = 4
c. European (E) Channels
   1. UHF (L), 471.25MHz (Ch. E21) : A = 11
   2. UHF (L), 470-660MHz (Except Ch. E21) : A = 12
   3. UHF (U), 660-890MHz : A = 16
d. American (A) Channels
   1. 471.25 to 507.25MHz (Ch. A14 to A20) : A = 9
   2. 513.25 to 561.25MHz (Ch. A21 to A29) : A = 10
   3. 567.25 to 621.25MHz (Ch. A30 to A39) : A = 11
   4. 627.25 to 675.25MHz (Ch. A40 to A48) : A = 12
   5. 681.25 to 729.25MHz (Ch. A49 to A57) : A = 13
   6. 735.25 to 783.25MHz (Ch. A58 to A66) :
      A = 14789.25 to 849.25MHz (Ch. A67 to A77) :
      A = 15
   7. 855.25 to 885.25MHz (Ch. A78 to A83) :
      A = 16

2.11.6.4 Monitoring

Refer to Circuit Diagram 3913 466 72930 Sh. 130-1.

Each of the IF output stages V4, V5, V6 is connected to the monitor assembly 3913 466 72930 via a 470-ohm resistor. Each signal is rectified and the resulting DC voltage is applied to one inverting input of an open-loop operational amplifier, A1. The non-inverting inputs have a reference voltage derived from potential dividers. For example, V4 output is rectified by V1, V2, C3 and applied to A1 at Pin 2; Pin 3 is held at the reference voltage derived from the potential divider R3, R4, R5.

When the oscillator output is normal, A1 outputs are low. These outputs are fed to a NOR gate, A2, whose output feeds the LED driver V7.

2.11.7 Maintenance

2.11.7.1 General

The Crystal Oscillator is supplied already set up and should require only a periodic check of frequency to ascertain correct operation and the amount of crystal ageing. No maintenance of the LED and driver is involved, except periodic checks that they are functioning.

2.11.7.2 Adjustment of Frequency

A frequency counter is required, locked to a standard receiver.

Notes:

1. The oscillator should have been powered for at least one hour before this adjustment is made.

2. One of the three output sockets should be free and a frequency measurement an be made here without disturbing the operation of the transmitter.

3. INT/EXT switch to be set to INT, or INT wire link connected.

The frequency is adjusted using a trimming tool such as Johnson/Airtronic A78764 or small screwdriver through the holes marked FINE FREQ and COARSE FREQ in the outer cover. If, for any reason it is not possible to obtain the correct frequency with FINE FREQ, then the coarse frequency control must be used. The Oscillator should remain powered at all times during this adjustment, which is as follows:

a. Remove the Crystal Oscillator from its position in the chassis after removing the two fixing screws.
b. Set the INT/EXT switch to INT, or connect the INT wire link.

c. Set the FINE FREQ control to mid-position.
d. The COARSE FREQ control is now accessible and may be adjusted. It should be possible to set the oscillator frequency to within 10Hz of the desired figure.
e. Re-install the unit.
f. Finally, set the frequency accurately by means of the FINE FREQ.

2.11.8 Setting-up Procedures

2.11.8.1 General

The following setting-up procedures are applicable to new un-tested units, or units which have been repaired following failure in service. After completing the procedures the unit should be installed in the system and final adjustments carried out to meet the overall system requirements.

2.11.8.2 Test Equipment Required

a. Frequency counter, locked to a standard receiver.
b. Calibrated thermocouple or some other temperature measuring equipment using a small sensing element.
c. Milli wattmeter with 50 ohm terminating element capable of measuring up to 3mW.
d. Voltmeter capable of measuring 1V DC.

2.11.8.3 Adjustment of Maximum Oven Current

Note

This should only be necessary after replacement of an oven heater transistor V9 or V10.

a. Remove R29 and R30.
b. Attach the +12V supply between the feedthrough capacitor labelled +12V OVEN and ground.
c. Attach the voltmeter across resistor R31 with the positive lead to the feedthrough capacitor.
d. Switch on the supply and select a resistor for R29 which gives a voltmeter reading of 0.40 to 0.45V with the oven at room temperature.
e. Remove this resistor and place it on one side.
f. Repeat for R30.
g. Switch off and solder in these selected resistors ensuring that they are fitted in their correct places.

Switch on and note that the voltmeter reading does not exceed 1.0V, i.e. a current of 1.0A, as the oven heats up. If heating from 20°C, the operating temperature of 75°C will be reached after about six minutes and the current will fall.

2.11.8.4 Adjustment of Oven Temperature

Note:

Replacement of any components in the bridge circuit R21 to R27 will entail checking and possible adjustment of oven temperature.

a. Remove one of the four screws which secure the oven lid to the oven body.
b. The sensing element of the temperature measuring equipment should be inserted into this threaded hole.
c. Attach the +12V supply between the feedthrough capacitor labelled +12V OVEN and ground.
d. witch on and allow the oven to heat for about 10 minutes.
e. Adjust the temperature to 75°C using the trimmer R22 (TEMP) .
f. Remove the sensing element and replace the lid fixing screw.
g. It will now probably be necessary to adjust the frequency as described in section 2.11.7.2, Adjustment of Frequency.

2.11.8.5 Adjustment of Output Level

The RF output level at sockets X1, X2 and X3 should be equal and at a level of 1mW -0mW/ +0.3mW when measured with a milli wattmeter with 50 ohm terminating element. The output at any one socket will increase slightly as the other two are loaded so the output should be measured at each socket in turn leaving the two remaining outlets unloaded. The output level may be adjusted by changing the AOT resistor R14, R16 or R18 associated with the output X1, X2 or X3 respectively. 150 ohm is a suitable starting value and should be fitted to all three outputs initially.

2.11.8.6 Adjustment of Oscillator After Component Replacement

The following adjustments may be necessary after an oscillator component replacement and will certainly be necessary after crystal replacement.

Notes :

1. If the crystal is being replaced with one of the same frequency AOT Capacitor C1 will be of the correct value as it is frequency conscious. If a crystal of different frequency is being substituted then the table of values for C1 shown on the circuit diagram should be referred to.

2. Capacitor C4, when fitted, is 12pF and mounted on tags so that it may be removed completely if the frequency is too low to be corrected by C3 (COARSE FREQ).

3. The type of capacitor used for C1 and C4 is important for optimum stability and should be of sintered silvered mica in a resin moulded case. Suitable types are Lemco MS 89/M/R, ITT 454-60.

4. Use a suitable trimming tool such as Johnson/Airtronic AT 8764 for adjusting trimmers C2 and C4.

a. Connect one RF output to a frequency counter locked to a standard receiver.
b. Connect a second RF output to a milli wattmeter with 50 ohm terminating element.
c. Attach +12V supplies to appropriate feedthrough capacitors labelled +12V OVEN and +12V OSC with negative to ground.
d. Allow 15 minutes for the oven to heat up and component temperatures to stabilise.
e. Set the fine frequency control R19 (FINE FREQ) to mid travel.

f. Adjust trimmer C2 accessible through the hole in the oven lid until maximum indication is obtained on the milli-wattmeter. The level should be at or near 1mW.
g. Check that the frequency is near to that required.
h. Adjust trimmer C3, accessible through the hole in the oven lid labelled COARSE FREQ, until the correct frequency is obtained.
i. If this proves not possible and the frequency is low, remove C4, 12pF and fitted on tags. If the frequency is too high firstly ensure that C4 is fitted and then increase C2 slightly by turning clockwise until the required frequency is obtained. Ensure that C3 is not at one extreme as this may leave nothing in hand to compensate for crystal ageing. Addition or removal of C4 may effect the amplitude.
j. Check that the oscillator re-starts after disrupting the supply voltage.
k. The Output Level must now be set as described in section 2.11.8.5, Adjustment of Output Level.
l. Replace the oven cover and outer covers. Check the frequency again after one hour to confirm.
m. If the crystal is new it will age quite rapidly and the frequency will require checking frequently for the first month.

Note:

Before putting the oscillator into use, ascertain whether it is to be under internal or external fine frequency control, and set the switch or wire-link connections as required.

2.12 Flywheel Sync Delay Assembly

2.12.1 General Description

The Flywheel Sync Delay Assembly prevents disturbances in the video signal from overdriving the RF amplifier stages by generating a mute signal for the video processor module.

To ensure that there is no loss of gain-control in the transition between “Video On” and “Video Off”, delayed sync pulses are also generated on this board, even when there is no video input. These delayed pulses are not full-specification sync pulses because they are only used to drive sampling circuits. Variable delay is achieved by varying the width of the pulse (the trailing edge is used to trigger the sample pulse generators).

2.12.2 Technical Description

Refer to circuit diagram 3913 467 12420 Sh. 130-1.

The composite sync signal is input to the board via X1 (SYNC IN). The signal is positive-going with a baseline at zero volts and an amplitude of 1V. V2 is an inverting buffer which is AC coupled to the input by C1. This configuration ensures that in the absence of sync pulses, the collector of V2 will stay high (+12V) even if the sync input rests at +1V.

A1A is a line sync separator. It is a non-re-triggerable 62µs monostable which is triggered on the leading edge of the sync pulse (negative-going edge at the collector of V2). The output from pin 6 of A1A is a train of 2µs pulses at the line frequency which is used to reference the phase detector of a line-locked phase locked loop in A2.

The oscillator in A2 runs at 64 times the line frequency (1MHz for PAL systems and 1.008MHz for NTSC). A3 is a divider which produces square waves at the line frequency when the loop is locked on pin 4. Pin 3 outputs pulses at twice the line frequency and pin 11 at 32 times the line frequency. These two outputs are connected to a D-type flip-flop (A5B) which produces a $^{1}/_{32}$ time-shifted output at twice the line frequency via pin 12.

A1B is a monostable which is triggered by the positive leading edge of the divide-by-64 locked-oscillator output. The monostable output pulse width is set by R10 and must be wider than the pulse produced by A4B.

A4B and A5A form a sync-width discriminator which is triggered by the input sync. If the input pulse stays low for longer than the monostable time (6µs) a low is clocked through A5A, and pin 1 goes low. This is the condition during the frame broad pulses, when the resulting pulse resets A4A (the output sync pulse generator) and so prevents the generation of pulses during this period.

A4A generates the output sync pulses, the width of which may be varied by R11 in order to trigger the sample pulse generators in the AGC circuits of the host transmitter.

To prevent an unwanted output pulse being generated during the transition from line 625 to line 1 in the frame broads, the triggering edge (negative-going) must be delayed by more than 6µs (the pulse width of A4B).

When there are no sync pulses at the input, pin 11 of A4B is high and pulses are input from the oscillator via pin 12; pin 1 of A5A is therefore high and an output pulse train is maintained at the output.

V5 buffers the CMOS IC and produces pulses of 1V into 75 ohms.

If the loop becomes unlocked for any reason, A2 pin 1 goes low turning on V1 to illuminate the LED and produce a high at the VIDEO MUTE output.

2.12.2.1 Technical Data

a. Input Pulse Amplitude : 1V into 75 ohm
b. Output Pulse : 1V into 75 ohm
c. Output Pulse Characteristics :
   Line frequency (No output during frame broads)
d. Delay Range:
   1. Leading Edge of Output Pulse : 6.5µs
   2. Trailing Edge of Output Pulse : 6.0µs
e. Video Mute Output(Unlock LED On) : +12V
f. Video Mute Output(Lock) : High impedance.
g. Power Supply : +12V, 50mA

2.12.3 Test Procedure

a. Connect a 12V power supply and, with no input connected, check that the Unlock LED is illuminated.
b. Connect a source of 1V sync pulses to X1 (sync input).

1. If the Unlock LED is not illuminated, then check the following pulse widths:
   a) TP1 :
      should be 62µs +1/-2µs. AOT R1 to achieve this. Starting value of R1 is 100 kilohms.
   b) TP2 :
      0V/12V inverted sync.
   c) TP3 :
      line frequency square wave (leading edge coincident with leading edge of input sync when loop locked). TP4 +12V when loop is locked.
   d) TP5 :
      twice line frequency delayed by ¼ of the line period
   e) TP6 :
      greater than 6µs adjustable by R10
   f) TP7 :
      6µs ±0.5µs
   g) TP8 :
      +12V for normal line syncs, 0V during frame broads.
   h) TP9:
      +6V when loop is locked.

c. Check the output sync on X2; it should be 1V when loaded with 75 ohm and the width variable using R11.

2.12.4 Setting Up Procedure In Transmitter

Checking the Timing of the Black Level Sample Pulse:

1. Ensure the delay through the Flywheel Sync Delay module has been set up correctly in the Exciter (refer to section 2.12.3).
2. In the Aural and Visual Corrector module, observe the waveforms on TP3 (Video) and TP7 (Pulse) and adjust R11 on the Flywheel Sync Delay for 1 to 1.5µs delay between the trailing edge and the leading edge of the timing pulse. The correct timing should coincide with minimal distortion of the frame blanking period at the Exciter output.

2.13 Harmonic Generator

2.13.1 General Description

This unit generates harmonics of the master oscillator output, from which a local oscillator frequency is derived to produce sound and vision RF outputs.

It accepts the master oscillator output at a nominal level of 1mW at a frequency in the range 42 to 58MHz, determined by final carrier frequency, and amplifies it to 500mW. The amplified signal is applied to an impulse generator based on a step-recovery diode, which converts the energy in each input cycle into a narrow pulse of large amplitude, rich in harmonics.

The impulse generator output is terminated in a resistive attenuator and produces a spectrum or ‘comb’ of frequencies spaced by the master oscillator fundamental. The desired harmonic is then selected by an external ‘comb-line’ filter and raised to the required level by a broad band distribution amplifier.

A test point for use with a DVM is provided to check the input match to the impulse generator.

2.13.2 Technical Data

a. Master Oscillator (Input X1) :
   1. Input Level : 1mW
   2. Frequency Range : 42 to 58.8MHz
   3. Input Impedance :
      50 ohms nominal, TNC connector
   4. Input VSWR : Not worse than 1.3.

b. Impulse Generator (Output X2) :
   1. Output level at the Required Harmonic :
      -8dBm to +4dBm
   2. Output Impedance :
      50 ohms nominal, TNC connector.

c. Multiplication Factor :
   a) 11 for Channel E21
   b) 12 for Channel E22 to E44
   c) 16 for Channel E45 to E58
   d) 9 for Channels A14 to A20
   e) 10 for Channels A21 to A29
   f) 11 for Channels A30 to A39
   g) 12 for Channels A4 0 to A48
   h) 13 for Channels A49 to A57
   i) 14 for Channels A58 to A66
   j) 15 for Channels A67 to A77
   k) 16 for Channels A78 to A 83

d. Power Supply : +24V at 470mA quiescent
   -12V at 10mA.

e. Monitoring :
   1. Optimum Impulse Generator Matching :
      Maximum voltage at TP1.

f. Internal DC Voltages :
   Refer to section 2.13.4, Setting up procedure.

g. Dimensions :
   Width : 170mm
   Height : 80mm
   Depth : 670mm

h. Weight : 0.9kg.

2.13.3 Technical Description

Refer to schematic 3913 467 13220 Sh 130-1.

The harmonic generator receives the output of the channel oscillator at a level of approximately 1mW, and amplifies and then multiplies the signal to produce an output which is between 0.16mW and 2.5mW, dependent on channel and multiplication.

For the purposes of description the unit can be divided into two sections:

- 500mW Amplifier.
- Impulse Generator and its bias arrangement.

2.13.3.1 500mW Amplifier

A1 is a modular thin-film hybrid amplifier of high reliability, using gold metalisation throughout. It accepts the master oscillator input at a nominal level of 1mW and raises it to 500mW.

As it has a bandwidth in excess of that required, a Zobel network C20, R14 is used on the intermediate stage to curtail the high-frequency response.

The amplifier operates in Class A and has a nominal 24V supply.

2.13.3.2 Impulse Generator

The function of the circuit is as follows. Step-recovery diode V2 is alternately forward- and reverse-biased by the two half-cycles of the input signal. When forward-biased its equivalent circuit is that of a large capacitance which charges via a stripline inductor. When the change from forward to reverse bias occurs there is a rapid transition to reverse-bias capacitance. The energy stored in the inductor appears across this capacitance immediately in the form of a narrow half-sine voltage pulse. Thus a sharp pulse with high harmonic content is produced.

C11 and C12 tune the inductor to resonance at the fundamental master oscillator frequency, thereby producing a substantially resistive impedance at that frequency and reflecting harmonics towards the output. This impedance is transformed to the output impedance of A1 by a two-stage matching network: the first (fixed) stage consists of C9, C10 and the inductor; the second (adjustable) stage consists of L5, C7, C8, C27. Thus the output of A1 is matched to the impedance of the impulse generator; this matching ensures maximum power applied to V2 and hence maximum possible level of high-order harmonics generated.

To facilitate adjustment of the matching a reflected power probe is inserted in the line between A1 output and the matching network. A sample from the probe is passed through the low-pass filter L4, C3, C4, C5 and detected by V1. The detected output may be monitored by a DVM measuring volts at TP1. C7 and C8 are adjusted to give a minimum reading indicating maximum power transfer to the impulse generator, and hence correct match.

The output of the impulse generator is terminated in the resistive network R7, R8 which enables a stable and fairly level ‘comb’ of frequencies to be generated from the output pulse.

To ensure that the transition from forward to reverse bias occurs at the correct point for maximum output it is necessary to apply a reverse bias to V2. Since V2 has to operate with its cathode grounded, for maximum heat dissipation, this bias is negative with respect to ground and is derived from the potential divider R9 (providing the bias adjustment), R10, R11. RF and low-frequency decoupling is provided by C19 and C18 on the RF printed board.

2.13.4 Setting-up Instructions

The following setting-up procedures are applicable to new untested units or units which have been repaired following their failure in service.

In some cases the procedures are sufficient only to ensure the correct functioning of the unit, in which case the unit should be put into or returned to service and the final adjustments carried out to give the required system performance.

2.13.4.1 Equipment Required

a. Power supply, +24V, 0.5A, current-limited.
   -12V, 0.1A, current-limited.
b. Crystal Oscillator 3913 466 40320
   OR
   Stable signal generator covering the range 42 to 59MHz and giving 1mW (0dBm) output, and frequency counter.
c. Comb line Filter 3913 467 14710(L)
   OR
   3913 467 14720(U)
d. RF power meter with 50 ohm 0.5W terminations.
e. RF spectrum analyser.
f. High impedance digital voltmeter.

2.13.4.2 Procedure

a. With all inputs and outputs terminated in 50 ohms, apply +24V to C26 and -12V to C27 and check that the current consumption of the unit does not exceed 500mA.
b. Set R9 to provide -4.2V bias to V2, as measured with a high-impedance meter at TP2.
c. Apply an input signal of the required frequency at 0dBm (1mW) to X1. The match of the amplifier to the impulse generator may be realised in one of the following three ways, the first being preferable.
   1. Connect X2 to the spectrum analyser with a wide enough sweep so that the complete harmonic spectrum may be viewed. Tune the matching variables C7 and C8 to obtain best match and hence highest level of Harmonics at X2. To obtain the best match it may be necessary to alternately increase C7 and decrease C8, or vice versa, once the tuning point is found. Slight adjustment of R9 may also prove necessary.
   2. Connect X2 to the appropriately tuned comb-line filter, and the output of the filter to the power meter. Adjust C7, C8 and if necessary, R9 as described in step c.1. to give maximum reading on the power meter.
   3. Terminate X2 with 50 ohm and connect the voltmeter to TP1. Adjust C7,C8 and if necessary, R9 as described in step c.1. to give a minimum reading on the meter.

2.13.4.3 Maintenance - General

If any component is replaced, ensure that lead lengths and position of the replacement component are as close as possible to the original ones. Module A1 is connected by printed circuit board sockets to enable it to be replaced easily. If it is necessary to replace V2, proceed as follows:

a. Remove the two M3 screws securing A1.
b. Remove the six M3 screws marked X on the assembly drawing and remove the heatsink.
c. Withdraw the diode mounting screw with the diode.
d. To fit the replacement diode first apply additional heat sink compound to the base of A1 and the diode mounting block if necessary and then follow steps (a) to (c) in reverse order.

Note:
The interface between the front plate which carries socket X1, and the remainder of the unit has been treated with a special conductive caulking compound. If this joint is broken, the spectral purity of the response of the unit will deteriorate.

2.13.4.4 Voltage Analysis

a. Power Supply :
   1. +24V, 470mA
   2. -12V, 10mA
b. Module A1:
   1. HT at C22 : 24.0V
   2. Pin 6 : 23.7V
   3. Pin 5 : 23.7V
   4. Pin 9 : 23.3V
c. V2 Anode : -3.3V to -5.0V

2.14 RF Distribution Amplifier (2 To 5-way)

2.14.1 General Description

The RF Distribution Amplifier or RF DA is an active splitter/amplifier used to supply more than one module with identical UHF signals.

Applications include UHF oscillator supply and UHF modulated TV distribution, providing up to five simultaneously level-controlled outputs.

In their construction the modules employ surface mount technology on a standard printed circuit board with integral UHF shield strip and cover. Output level adjustment is controlled via a hole in the shield cover.

2.14.2 Technical Data

a. Input Impedance : 50 ohm
b. Return Loss : 1dB, 400 to 900MHz.
c. Input Level :1mW CW or peak sync nominal
d. Output Impedance : 50 ohm
e. Output Level Control Range : 40dB
f. Gain For 2 Output Version : 24dB
g. Gain For 3 Output Version :21dB
h. Gain For 4 Output Version : 19dB
i. Gain For 5 Output Version : 17dB
j. Supply Requirements :
   +12V, 600mA max for 5 outputs.

2.14.3 Technical Description

Refer to drawing 3913 466 78060 Sh.130-1.

The RF DA is an expandable module allowing a combination of UHF outputs to be realised. By selecting the number of hybrid amplifiers and value of the corresponding resistive splitter, 2 to 5 outputs may be selected at assembly.

The combined UHF signal at a nominal 1mW peak sync enters the module via X1. It passes through a PI matching section R1, R2, R3 before being amplified by V3 and its associated components. This stage provides a fixed gain of approximately 8dB.

The signal is then applied to the variable attenuator A6. The attenuator has a range of approximately 40dB and is controlled via potentiometer R12.

The attenuation controlled signal then passes through an even splitter network R7, R8, R9, R10, R25 whose values are dependent on the number of outputs required.

The signals from the splitter are amplified separately by A1 to A5, having a nominal 1dB pass band ripple, and a fixed gain of 28dB.

The theoretically obtainable maximum gain figures for possible configurations are shown in the Table 2-7.

Provision for a second PI (Attenuator/ matching section) is provided on all outputs.

2.14.4 Setting-up Procedure

The following setting-up procedure is applicable to new untested units, or units which have been repaired following failure in service. After completing the procedure the unit should be installed in the system and final adjustments carried out to meet the overall system requirements.

2.14.4.1 Test Equipment

a. Power Supply : +12V stabilised, 1A.
b. UHF Signal Generator and Power Meter
   or
   Network Analyser.

2.14.4.2 Procedure

As the unit functions only as an amplifying block the test procedure only checks for correct gain levels for a given configuration and input signal.

a. Apply a nominal 1mW CW mid-band UHF signal to

5 Amplifiers	18dB
4 Amplifiers	20dB
3 Amplifiers	22dB

Table 2-7 Theoretical Gain Figures

X1.

b. Connect a power meter to X2. Turn the GAIN control R12 fully clockwise. Check that the level corresponds to a gain consistent with that shown in Table 2-7 for the amplifier configuration under test.
c. Alternatively, use a network analyser to check the level at X2.
d. Repeat (b) or (c) for the remaining outputs and check that all outputs are within 1dB of each other when one output is set to 0dBm.

2.15 RF Distribution Amplifier (Local Oscillator)

2.15.1 Technical Description

Refer to Circuit Diagram 3913 467 14650 Sh 130-1.

The RF DA is used in drive and other low-level circuits requiring a single UHF signal be distributed to several points. The DA operates with an input level of approximately 1mW and can have a maximum gain of 20dB to four separate outputs. Unused outputs are terminated.

The combined UHF signal at a nominal 1mW peak sync enters the module via X1. It passes through a PI matching section R1, R2, R3 before being amplified by V3 and its associated components. This stage provides a fixed gain of approximately 8dB.

The signal is then applied to the variable attenuator A6. The attenuator has a range of approximately 40dB and is controlled via potentiometer R12.

The attenuation controlled signal then passes through an even splitter network R7, R8, R9, R10. The signals from the splitter are amplified separately by A1 to A4, having a nominal 1dB pass band ripple, and a fixed gain of 28dB.

The theoretically obtainable maximum gain to each output is 20dB. Provision for a second PI matching section is provided on all outputs.

The output level from the RF distribution amplifier is set to 5mW and 12mW.

2.15.2 Setting Up Procedure

The following setting-up procedure is applicable to new untested units, or units which have been repaired following failure in service. After completing the procedure the unit should be installed in the system and final adjustments carried out to meet the overall system requirements.

2.15.2.1 Test Equipment

a. Power Supply: +12V stabilised, 1A.
b. UHF Signal Generator and Power Meter or Network Analyser.

2.15.2.2 Procedure

Since the unit functions only as an amplifying block the test procedure checks only for correct gain levels for a given configuration and input signal.

a. Apply a nominal 1mW CW mid-band UHF signal to X1.
b. Connect a power meter to X2. Adjust the GAIN control R12 throughout its range. Check that at approximately mid range the output on X2 is 5mW.
c. Alternatively, use a network analyser to check the level at X2.
d. Connect the power meter to X3. Check that the output is within 1dB of the output on X2.
e. Check that the outputs on X4 and X5 are 3dB up on X2.

2.16 Comb Line Filter Assembly

2.16.1 General Description

2.16.1.1 Introduction

Comb Line Filter Assemblies 3913 46714710 (L) and 3913 467 14720 (U), between them cover the complete UHF TV Bands. They are employed as:

a. A Local Oscillator Filter
   To select the required harmonic frequency from the output of the harmonic generator, attenuating all unwanted harmonics by at least 60dB.
b. A Channel Filter
   To select the wanted sideband at the output of the 50mW mixer/amplifier assembly and suppress the unwanted sideband and local oscillator frequencies by at least 60dB.

2.16.1.2 Construction

Refer to Figure 2-41. Both filters are similar in construction, although they differ slightly in overall size. They are built in fabricated rectangular boxes and have four tuned resonant rods, tuned by means of tuning screws which capacitively load the open ends of the rods. The input and output couplings are made via spring contacts which slide along the two outer rods and which are attached to female TNC coaxial connectors on the ends of the box. By varying the position of the connector the coupling is adjusted.

2.16.2 Technical Data

2.16.2.1 Filter Assembly 3913 467 14710 (L)

a. Frequency Range : 470 - 696MHz
b. Channels Covered :
   1. American A14 - A45
   2. European E21 - E44
c. Bandwidth :
   1. 470 - 665MHz :

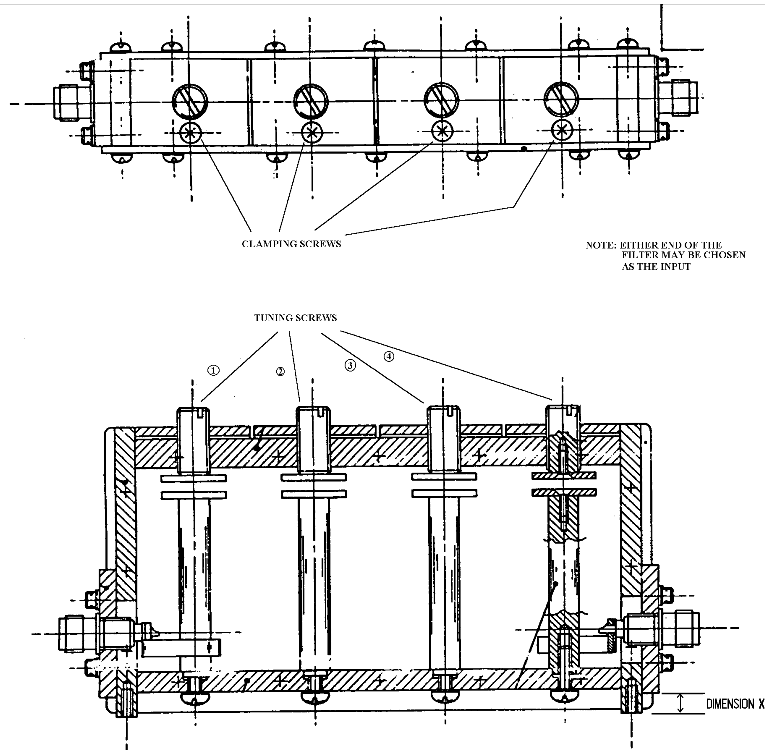


Figure 2-41 Filter Assembly Details

   a) 8MHz minimum at -0.5dB
   b) 75MHz maximum at -60dB
2. 665 - 695MHz :
   a) 7MHz minimum at -0.5dB
   b) 5MHz maximum at -60dB

d. Input VSWR :
1. 470 - 665MHz :
   a) Band centre ±2.75MHz better than 1.1
   b) Band centre ±3.5MHz better than 1.2
2. 665 - 696MHz :
   a) Band centre ±2.5MHz better than 1.1
   b) Band centre ±2.75MHz better than 1.2

e. Pass band Insertion Loss : less than 1.0dB

f. Impedance : 50 ohms TNC connectors

g. Overall Dimensions :
55 x 120 x 190 mm inclusive of sockets and mounting brackets.

h. Weight : 1,140 g.

2.16.2.2 Filter Assembly 3913 467 14720 (U)

a. Frequency Range :
650 - 930MHz

b. Channels Covered :
1. American A46 - A83
2. European E45 - E72

c. Bandwidth :
1. 8MHz minimum at -0.5dB
2. 75MHz maximum at -60dB

d. Input VSWR :
1. 650 - 890MHz :
   a) Band centre ±2.75MHz better than 1.1
   b) Band centre ±3.5MHz better than 1.2
2. 890 - 930MHz :
   a) Band centre ±2.5MHz better than 1.1
   b) Band centre ±3.2MHz better than 1.2

e. Pass band Insertion Loss :
Less than 1.0dB

f. Impedance : 50 ohms TNC connectors

g. Overall Dimensions : 55 x 120 x 190mm inclusive of sockets and mounting brackets.

h. Weight : 1,030 g.

2.16.3 Maintenance

2.16.3.1 General

The comb line filters are supplied already set up and under normal circumstances should not require further adjustment. In the event of the setting of a filter being disturbed it may be re-aligned by means of the following procedure.

2.16.3.2 Alignment Procedure

a. Using the vision carrier frequency, f_v, and the local oscillator frequency, f_o, find the passband centre frequency, f_c, to which the filter will be set:
1. For the local oscillator filters : $f_c = f_o$
2. For the channel filters (Vision and Sound) :
$f_c = f_v + 2MHz$

b. The input and output couplings should now be roughly set. This is done by adjusting both socket assemblies on the filter to give the correct Dimension "X" as calculated by one of the following formulas:

   1. For the lower band filter 3913 467 14710, Dimension "X" (mm) = 0.025 (890-f_c)
   2. For the upper band filter 3913 467 14720, Dimension "X" (mm) = 0.0117 (1207-f_c)
      where: f_c is in MHz.
      Dimension "X" is measured from the bottom of the end plate to the bottom of the socket assembly as shown on Figure 2-41.

c. Referring again to Figure 2-41, it can be seen that associated with each tuning screw there is a clamping screw. Tighten these sufficiently to prevent free rotation of the tuning screws but not so much as to prevent adjustment by means of a suitable screwdriver.

d. Turn the four tuning screws fully in.

e. Arrange test equipment and filter as shown on Figure 2-42.

f. Display the return loss, or VSWR, as measured at the filter input over the frequency range ±10MHz approximately.

g. Adjust tuning screw 1 until a spike, or ripple, is seen on the display. This should be centred on f_c.

Note

This spike, or ripple, will be quite small and to avoid missing it the test equipment should be set to maximum sensitivity.

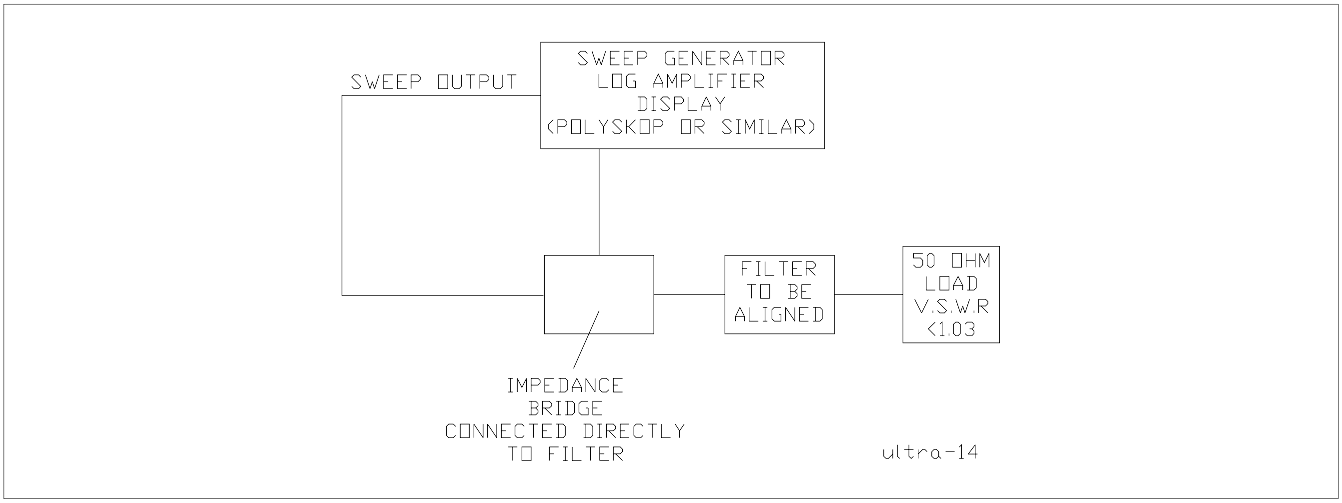


Figure 2-42 Filter Alignment Set-up

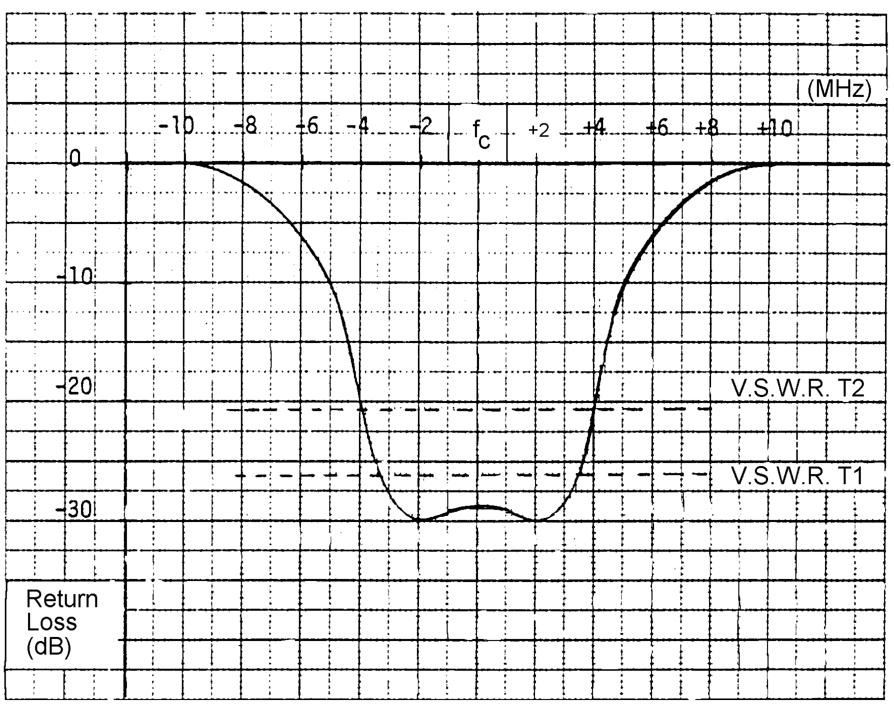


Figure 2-43 Typical Input VSWR

h. Adjust tuning screw 2 until the spike, or ripple, widens and/or deepens.

i. Carefully adjust tuning screw 2 and, if necessary, tuning screw 1, to give as symmetrical a response as possible centred on f_c.

j. Adjust tuning screw 3 until the response widens and/or deepens.

k. Carefully adjust tuning screw 3, and if necessary, tuning screws 1 and 2 to give as symmetrical a response as possible centred on f_c.

l. Adjust tuning screw 4 until the response widens and/or deepens.

m. Adjust each of the tuning screws as necessary, and the input and output couplings to give the specified input match conditions. A typical result is shown in Figure 2-43.

n. Check that the amplitude/frequency response complies with the specification.

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Replaceable Parts List Index

Table 3-1. EXCTR SIGMA 470-662 M MONO - 8928 117 31310

HARRIS P/N	DESCRIPTION	QTY/UM	REF. SYMBOLS/EXPLANATIONS
939 8121 582	CHASSIS EXCITER	1.0 EA	
952 9190 286	C/F IOT EXCITER	1.0 EA	
952 9190 287	KIT OF COAX CABLES	1.0 EA	
3913 466 2480001	VIDEO PROC FOR M/N SYSTEMS	1.0 EA	0025
3913 466 2483006	GRP DLY 2-45.75MHZ SYS M/N	1.0 EA	0027
3913 467 14710	COMBLINE FILTER BND4	2.0 EA	
992 9413 001	MOD/VSB ASSY SYS M	1.0 EA	0035
3913 466 2481001	RX GRP DLY P1 CURVE	1.0 EA	0037
3913 466 37970	DIFF.PHASE CORRECTOR ASSY	1.0 EA	0040
992 9737 021	AURAL/VISUAL CORRECTOR	1.0 EA	
992 9737 095	AURAL CORRECTOR ASSY	1.0 EA	
3913 467 13260	COMBINED MIXER/UP CONVERTER	1.0 EA	
3913 467 12420	FLYWHEEL SYNC DELAY ASSY	1.0 EA	
4313 466 4032402	XSTAL OSC - 45.75MHz IF	1.0 EA	0060
4313 466 4032403	XSTAL OSC - CHANNEL	1.0 EA	0065
3913 467 13220	HARMONIC GENERATOR	1.0 EA	
3913 467 13940	SOUND MODULATOR	1.0 EA	075
3913 466 78060	PCB-RF DIST AMP 3 WAY	1.0 EA	
922 1206 254	LABEL EXCITER	1.0 EA	
3913 467 14650	RF DIST AMP PCB 4WAY (ULTRA)	1.0 EA	
8213 268 79059	ADPT RF TNC ELBOW	1.0 EA	0100
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	20.0 EA	0110
2522 178 15079	SCR PNPZ ST 18-8 M4 X 6	4.0 EA	0115
@PN = 2513 712 02004	**WSH CRKL ST 18-8 M3**	**24.0 EA**	0120
2513 712 02005	WSH CRKL ST 18-8 M4	13.0 EA	0125
430 0189 000	FAN AXIAL 24VDC 119x119x38mm	1.0 EA	0130
430 0192 000	GUARD FAN 119x119mm	2.0 EA	0135
2322 156 14708	RES 4R7 1% 0W6 MTLFLM	1.0 EA	R001
2000 003 06222	CAP 2200U 40V ELEC AX 105deg	2.0 EA	C001:C002
2413 015 01017	TERM INSUL DBLE M3 NUT	4.0 EA	
2522 178 15056	SCR PNPZ ST 18-8 M3 X 4	4.0 EA	
2522 178 15083	SCR PNPZ ST 18-8 M4 X 12	9.0 EA	
2522 600 79026	WSH PLN FRM A ST 18-8 M4	9.0 EA	
2422 015 01003	SOLDERTAG M4 SNGL BR SN	2.0 EA	
2522 401 50008	NUT FULL HEX ST 18-8 M3	6.0 EA	
2522 178 15062	SCR PNPZ ST 18-8 M3 X 12	6.0 EA	
8213 268 79189	WSH INSUL RF (BNC/TNC)	4.0 EA	
3913 080 54110	SPCR HEX TP M/F M3X25 BR	2.0 EA	
2422 015 09256	GROMMET PVC 6.4X1.6X 4.8	1.0 EA	
2522 178 15105	SCR PNPZ ST 18-8 M5X10	2.0 EA	
2513 712 02006	WSH CRKL ST 18-8 M5	2.0 EA	
2522 179 09094	SCR CSKPZ ST 18-8 M3	2.0 EA	
2413 015 06312	GROMMET PVC 9.5X3.2X 7.9	2.0 EA	
2422 026 03386	PLUG 3 WAY AUDIO FIXED	1.0 EA	
3913 080 54310	SPCR HEX TP M/F M3X30 BR	6.0 EA	

Table 3-2. EXCTR SIGMA 662-860 M MONO - 8928 117 31320

HARRIS P/N	DESCRIPTION	QTY/UM	REF. SYMBOLS/EXPLANATIONS
@PN = 939 8121 582	**CHASSIS EXCITER**	**1.0 EA**	
952 9190 286	C/F IOT EXCITER	1.0 EA	
952 9190 287	KIT OF COAX CABLES	1.0 EA	
3913 466 2480001	VIDEO PROC FOR M/N SYSTEMS	1.0 EA	0025

3913 466 2483006	GRP DLY 2-45.75MHZ SYS M/N	1.0 EA	0027
3913 467 14720	COMBLINE FILTER BND5	2.0 EA	
992 9413 001	MOD/VSB ASSY SYS M	1.0 EA	0035
3913 466 2481001	RX GRP DLY P1 CURVE	1.0 EA	0037
3913 466 37970	DIFF.PHASE CORRECTOR ASSY	1.0 EA	0040
992 9737 021	AURAL/VISUAL CORRECTOR	1.0 EA	
992 9737 095	AURAL CORRECTOR ASSY	1.0 EA	
3913 467 13260	COMBINED MIXER/UP CONVERTER	1.0 EA	
3913 467 12420	FLYWHEEL SYNC DELAY ASSY	1.0 EA	
4313 466 4032402	XSTAL OSC - 45.75MHz IF	1.0 EA	0060
4313 466 4032403	XSTAL OSC - CHANNEL	1.0 EA	0065
3913 467 13220	HARMONIC GENERATOR	1.0 EA	
3913 467 13940	SOUND MODULATOR	1.0 EA	075
3913 466 78060	PCB-RF DIST AMP 3 WAY	2.0 EA	
922 1206 254	LABEL EXCITER	1.0 EA	
8213 268 79059	ADPT RF TNC ELBOW	1.0 EA	0100
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	20.0 EA	0110
2522 178 15079	SCR PNPZ ST 18-8 M4 X 6	4.0 EA	0115
2513 712 02004	WSH CRKL ST 18-8 M3	26.0 EA	0120
2513 712 02005	WSH CRKL ST 18-8 M4	13.0 EA	0125
430 0189 000	FAN AXIAL 24VDC 119x119x38mm	1.0 EA	0130
430 0192 000	GUARD FAN 119x119mm	2.0 EA	0135
@PN = 2322 156 14708	**RES 4R7 1% 0W6 MTLFLM**	**1.0 EA**	R001
2000 003 06222	CAP 2200U 40V ELEC AX 105deg	2.0 EA	C001:C002
2413 015 01017	TERM INSUL DBLE M3 NUT	4.0 EA	
2522 178 15056	SCR PNPZ ST 18-8 M3 X 4	4.0 EA	
2522 178 15083	SCR PNPZ ST 18-8 M4 X 12	9.0 EA	
2522 600 79026	WSH PLN FRM A ST 18-8 M4	9.0 EA	
2422 015 01003	SOLDERTAG M4 SNGL BR SN	2.0 EA	
2522 401 50008	NUT FULL HEX ST 18-8 M3	8.0 EA	
2522 178 15062	SCR PNPZ ST 18-8 M3 X 12	6.0 EA	
8213 268 79189	WSH INSUL RF (BNC/TNC)	4.0 EA	
3913 080 54310	SPCR HEX TP M/F M3X30 BR	6.0 EA	
3913 080 54110	SPCR HEX TP M/F M3X25 BR	2.0 EA	
2422 015 09256	GROMMET PVC 6.4X1.6X 4.8	1.0 EA	
2522 178 15105	SCR PNPZ ST 18-8 M5X10	2.0 EA	
2513 712 02006	WSH CRKL ST 18-8 M5	2.0 EA	
2522 179 09094	SCR CSKPZ ST 18-8 M3	2.0 EA	
2413 015 06312	GROMMET PVC 9.5X3.2X 7.9	2.0 EA	
2422 026 03386	PLUG 3 WAY AUDIO FIXED	1.0 EA	

Table 3-3. VIDEO PROC FOR M/N SYSTEMS - 3913 466 2480001

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 2480000	VIDEO PROC ASSY	1.0 EA	
3913 466 7242001	PCB - VIDEO PROC SYS M/N	1.0 EA	0060

Table 3-4. VIDEO PROC ASSY - 3913 466 2480000

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
@PN = 3913 466 78360	**BAR TILT COMPENSATOR/HF BOOST**	**1.0 EA**	0003
3913 466 73490	PCB ASSY - PULSER MODIFI*	1.0 EA	001
3913 467 05400	CASE (VIDEO PROCESSOR)	1.0 EA	004
3913 463 82970	PWB MOUNTING BRACKET	1.0 EA	007
3913 461 48260	CONNECTOR MTG PLATE(INS)	1.0 EA	015
2422 034 16776	CONTACT SKT 22-20 AWG	7.0 EA	016

2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	2.0 EA	017
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	7.0 EA	022
2522 178 15038	SCR PNPZ ST 18-8 M2 X 6	1.0 EA	027
2513 712 02003	WSH CRKL ST 18-8 M2.5	2.0 EA	032
2522 401 60064	NUT FULL HEX ST 18-8 M2	2.0 EA	033
2522 178 15039	SCR PNPZ ST 18-8 M2.5	2.0 EA	034
2413 015 01384	TAG SOLDER 2BA	5.0 PK	035 040
9390 253 60765	LED MTG KIT SIZE T1 3/4	1.0 EA	041
3913 081 66620	MOD RECORD PLATE 1 TO 12	1.0 EA	043
3913 935 00009	REG 7815 +15V 1.5A TO-220	1.0 EA	A011
9332 897 10682	LED 5MM HLMP-3507 GRN	1.0 EA	H001
2432 020 00234	PLUG RF SMB 50R B/H SLDR	5.0 EA	X001 X002 X003 X004 X010
2422 025 02804	SKT 12 WAY (QIKMATE)	1.0 EA	X005
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	1.0 EA	C104
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	1.0 EA	026
2522 401 50008	NUT FULL HEX ST 18-8 M3	1.0 EA	027
2513 712 02004	WSH CRKL ST 18-8 M3	1.0 EA	042
@PN = 0722 102 48006	**CBL RF 75R RG179B/U TO MIL-C-1**	**0.50 RL**	055
3913 466 27270	TERMINATION ASSY - 75R	1.0 EA	071
0722 102 48006	CBL RF 75R RG179B/U TO MIL-C-1	1.20 RL	072

Table 3-5. PCB - VIDEO PROC SYS M/N - 3913 466 7242001

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 7242000	PCB ASSY - VIDEO PROCESS*	1.0 EA	0010 0015 0015
2222 682 34101	CAP 100P 2% 100V N150 0.1"	1.0 EA	C023

Table 3-6. PCB ASSY - VIDEO PROCESS* - 3913 466 7242000

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	35.0 EA	
3913 461 72420	PCB - VIDEO PROCESSOR	1.0 EA	001
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	19.0 EA	007
9390 125 10872	HEATSINK 5F (T0-5 x 12.7mm)	2.0 EA	008
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	2.0 EA	010
2522 401 50008	NUT FULL HEX ST 18-8 M3	2.0 EA	011
2513 712 02004	WSH CRKL ST 18-8 M3	2.0 EA	012
2413 024 00425	SKT 1 WAY PCB 2.16MM DIA	6.0 EA	013
9334 461 50749	IC LF356N	1.0 EA	A001
9332 775 90602	IC HEF4011BP	1.0 EA	A002
9333 243 30602	IC HEF4528BP	3.0 EA	A003 A009 A010
9336 240 00682	IC LM319N	2.0 EA	A004 A006
9333 905 60749	IC LM348N (DIL-14	1.0 EA	A005
9332 776 10602	IC HEF4013BP	1.0 EA	A007
9332 247 50749	IC LM741CN (DIL-8)	1.0 EA	A008
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	18.0 EA	C001 C002 C007 C008 C010 C012 C020 C024 C026 C029 C030 C033 C034 C035 C037 C047 C052 C053
2000 001 00002	CAP 10U 63V ELEC RADIAL	5.0 EA	C003 C004 C025 C042 C046 C048 C051
2222 682 34279	CAP 27P 2% 100V N150 0.1"	3.0 EA	C006C027 C028
2222 682 34121	CAP 120P 2% 100V N150 0.1"	2.0 EA	C009 C036
2012 310 00312	CAP 10N 20% 100V PSTR 0.2" P	1.0 EA	C013
2222 682 34399	CAP 39P 2% 100V N150 0.1"	1.0 EA	C014
2222 809 09003	CAP 2P0 - 18P TRIM (18E)	2.0 EA	C015 C016
2222 630 18391	CAP 390P 10% 100V MED-K 0.1"	1.0 EA	C017 AOT 220P-470P
2222 682 09478	CAP 4P7 0.25PF 100V NPO 0.1"	1.0 EA	C018
2222 682 09188	CAP 1P8 0.25PF 100V NPO 0.1"	2.0 EA	C019 C054

2222 682 34101	CAP 100P 2% 100V N150 0.1"	1.0 EA	C022
2000 300 00006	CAP 1N5 5% 100V PCRB RAD	1.0 EA	C031
2000 300 00003	CAP 470P 10% 100V PCRB RAD	2.0 EA	C032 C041
2222 630 18222	CAP 2N2 10% 100V MED-K 0.1"	1.0 EA	C038
2013 554 91701	CAP 180P 2% 100V CER	1.0 EA	C039
2222 809 08002	CAP 4P0 - 37P TRIM (37E)	3.0 EA	C040 C045 C050
2222 682 34689	CAP 68P 2% 100V N150 0.1"	2.0 EA	C043 C044
2000 300 00002	CAP 220P 5% 100V PCRB RAD	1.0 EA	C049
3913 076 50040	DELAY LINE 500NS TO SPEC*	1.0 EA	D001
@PN = 3913 469 50140	**CHOKE RF (6 HOLE FORMER)**	**2.0 EA**	
			L006 L007
3913 469 51370	COIL 34.2-37.8UH	1.0 EA	L004
3913 469 50280	COIL 17.1-18.9UH	1.0 EA	L005
2322 156 14701	RES 470R 1% 0W6 MTLFLM	6.0 EA	R002 R006 R007 R056 R101 R119
2322 156 11002	RES 1K 1% 0W6 MTLFLM	24.0 EA	R003 R004 R016 R019 R025 R028 R050 R061 R064 R066 R074 R079 R083 R084 R089 R100 R105 R111 R117 R118 R122 R123 R124 R128
2322 241 13106	RES 10M 5% 0W25 MTLGLZ	3.0 EA	R005 R013 R027
2322 156 18209	RES 82R 1% 0W6 MTLFLM	3.0 EA	R008 R010 R017
2122 350 00371	POT 100R 10% LIN W5 SIDE ADJ	1.0 EA	R009
2322 156 12701	RES 270R 1% 0W6 MTLFLM	3.0 EA	R011 R022 R026
2322 156 12201	RES 220R 1% 0W6 MTLFLM	6.0 EA	R012 R014 R023 R024 R048 R055
2322 156 11001	RES 100R 1% 0W6 MTLFLM	3.0 EA	R015 R039 R129
2322 156 12209	RES 22R 1% 0W6 MTLFLM	1.0 EA	R018
2322 156 11003	RES 10K 1% 0W6 MTLFLM	17.0 EA	R020 R029 R032 R041 R073 R078 R088 R091 R098 R109 R110 R114 R115 R125 R132 R133 R134
2322 156 11004	RES 100K 1% 0W6 MTLFLM	4.0 EA	R021 R077 R082 R130
2322 156 14702	RES 4K7 1% 0W6 MTLFLM	6.0 EA	R030 R040 R044 R051 R059 R068
2322 156 12002	RES 2K 1% 0W6 MTLFLM	3.0 EA	R031 R037 R090
2322 156 11602	RES 1K6 1% 0W6 MTLFLM	3.0 EA	R033 R034 R036
2322 156 12001	RES 200R 1% 0W6 MTLFLM	1.0 EA	R035
2322 156 13303	RES 33K 1% 0W6 MTLFLM	1.0 EA	R038
2122 350 00362	POT 100K 20% LIN W5	1.0 EA	R042
2322 156 15102	RES 5K1 1% 0W6 MTLFLM	1.0 EA	R043
2322 156 14302	RES 4K3 1% 0W6 MTLFLM	1.0 EA	R045
2122 350 00372	POT 5K0 10% LIN W5 SIDE ADJ	1.0 EA	R046
2322 156 11801	RES 180R 1% 0W6 MTLFLM	1.0 EA	R047
@PN = 2322 156 16809	**RES 68R 1% 0W6 MTLFLM**	**1.0 EA**	
			R049
2322 156 11202	RES 1K2 1% 0W6 MTLFLM	2.0 EA	R052 R116
2322 156 16801	RES 680R 1% 0W6 MTLFLM	3.0 EA	R053 R058 R099
2322 156 12202	RES 2K2 1% 0W6 MTLFLM	3.0 EA	R054
2322 156 12202	RES 2K2 1% 0W6 MTLFLM	3.0 EA	R057 R108
2122 350 00515	POT 1K0 20% LIN W5	1.0 EA	R060
2322 156 13602	RES 3K6 1% 0W6 MTLFLM	1.0 EA	R135
2322 156 15602	RES 5K6 1% 0W6 MTLFLM	1.0 EA	R063 A.O.T COMP
2322 156 11502	RES 1K5 1% 0W6 MTLFLM	1.0 EA	R065
2322 156 16802	RES 6K8 1% 0W6 MTLFLM	4.0 EA	R067 R075 R076 R092
2322 156 12009	RES 20R 1% 0W6 MTLFLM	1.0 EA	R069
2322 156 13909	RES 39R 1% 0W6 MTLFLM	1.0 EA	R070 A.O.T COMP
2322 156 17509	RES 75R 1% 0W6 MTLFLM	2.0 EA	R071 R072
2322 156 15101	RES 510R 1% 0W6 MTLFLM	1.0 EA	R080
2322 241 13475	RES 4M7 5% 0W25 MTLGLZ	1.0 EA	R081
2322 156 11203	RES 12K 1% 0W6 MTLFLM	5.0 EA	R085 R095 R097 R102 R113
2322 156 15603	RES 56K 1% 0W6 MTLFLM	2.0 EA	R086 R106

2122 350 00354	POT 1K0 20% LIN W5	2.0 EA	R087 R121
2322 156 11803	RES 18K 1% 0W6 MTLFLM	1.0 EA	R093
2322 156 13301	RES 330R 1% 0W6 MTLFLM	1.0 EA	R094
2322 156 11503	RES 15K 1% 0W6 MTLFLM	1.0 EA	R096
2322 156 12403	RES 24K 1% 0W6 MTLFLM	1.0 EA	R103
2322 156 16201	RES 620R 1% 0W6 MTLFLM	1.0 EA	R104
2322 156 14703	RES 47K 1% 0W6 MTLFLM	1.0 EA	R107
2122 350 00363	POT 5K0 20% LIN W5	1.0 EA	R126
2322 156 15109	RES 51R 1% 0W6 MTLFLM	1.0 EA	R131
9335 639 70715	TRANS U441	2.0 EA	ALT.SEE ‘R’ SHT. V001 V016
9331 177 90112	DIODE BZX79C10	3.0 EA	
@RD = V002 V031 V039			
9330 295 71112	TRANS 2N2369A	2.0 EA	V003 V054
9331 977 10112	TRANS BC557	7.0 EA	V004 V009 V019 V021 V022 V035 V045
9330 473 10112	DIODE 1N916	11.0 EA	V005 V008 V032 V033 V034 V037 V040 V041 V042 V043 V044
9330 226 40112	TRANS 2N2905	1.0 EA	V006
9330 282 80112	TRANS 2N2219	1.0 EA	V007
9330 566 80112	TRANS BCY89	1.0 EA	V010
9331 976 10112	TRANS BC547	7.0 EA	V011 V017 V018 V020 V023 V024 V025
9331 178 20112	DIODE BZX79C13	2.0 EA	V012 V028
9332 533 70682	TRANS SD211DE	3.0 EA	V013 V029 V046
9336 814 30112	TRANS BSD214	6.0 EA	V014 V015 V030 V047 V051 V057
9336 508 80682	TRANS BS250 (TO-92)	2.0 EA	V026 V058
9336 619 30682	TRANS 2SK216	1.0 EA	V027
9331 177 80112	DIODE BZX79C9V1	1.0 EA	V038
9333 341 80112	DIODE BAX12A	5.0 EA	V048 V049 V050 V052 V055
9334 146 80112	DIODE BZX79C2V4	1.0 EA	V053
9338 827 27682	DIODE BAT48 (DO-35)	1.0 EA	V056
2413 490 00001	SPACER TO5-001	2.0 EA	FIT WITH V6 & V7
2322 156 17502	RES 7K5 1% 0W6 MTLFLM	1.0 EA	R112
2322 156 18201	RES 820R 1% 0W6 MTLFLM	1.0 EA	R120
2322 156 11002	RES 1K 1% 0W6 MTLFLM	1.0 EA	R127
2413 535 00199	CHOKE 33UH 0W33 BS9751-N0001-C	1.0 EA	L008
2222 683 34689	CAP 68P 2% 100V N150 0.2"	1.0 EA	C055
2400 545 10026	BEAD FXD 3.5X1.2X3MM F14	2.0 EA	USE WITH V026:V058
492 0872 000	CHOKE, 0.33MH 1.25 OHM	3.0 EA	L001:L002:L003
522 0649 000	CAP 470UF 35V 20%	3.0 EA	C021:C005:C011

@T = BAR TILT COMPENSATOR/HF BOOST - 3913 466 78360

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 461 78360	PCB BAR TILT COMPENSATOR/HF BO	1.0 EA	0001
2400 040 10056	PIN - EYELET MOUNT	3.0 EA	0002
2513 621 98476	EYELET 1.6MM O/D X 3.7MM BRSS	3.0 EA	0003
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	2.0 EA	0004
2222 683 09828	CAP 8P2 0.25PF 100V NPO 0.2"	1.0 EA	C001: A O T 2-18PF
2000 501 01568	CAP 5P6 0P5 50V NPO CER 1206	1.0 EA	C002
2000 501 04333	CAP 33N 10% 50V X7R CER 1206	1.0 EA	C003
3913 469 51400	COIL 58.9-65.1UH	1.0 EA	L001
2122 350 00459	POT 10K 10% LIN W5 SIDE ADJ	1.0 EA	R001
2122 350 00515	POT 1K0 20% LIN W5	1.0 EA	R002
2100 700 05222	RES 2K2 5% 0.25W Size 1206	1.0 EA	R003
2422 549 26016	SKT 2 WAY 2.54MM PITCH	1.0 EA	0005
3913 445 50120	HEADER 1 X 3	1.0 EA	X001

Table 3-7. PCB ASSY - PULSER MODIFI* - 3913 466 73490

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 461 73490	PCB - PULSER MODIFICATION	1.0 EA	001
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	9.0 EA	002
3913 445 50120	HEADER 1 X 3	1.0 EA	003
2422 549 26016	SKT 2 WAY 2.54MM PITCH	1.0 EA	004
2000 001 00002	CAP 10U 63V ELEC RADIAL	1.0 EA	C001
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	1.0 EA	C002
@PN = 2322 156 11009	**RES 10R 1% 0W6 MTLFLM**	**1.0 EA**	
			R001
2322 156 13301	RES 330R 1% 0W6 MTLFLM	1.0 EA	R002
2322 156 17509	RES 75R 1% 0W6 MTLFLM	1.0 EA	R003
2322 156 11004	RES 100K 1% 0W6 MTLFLM	1.0 EA	R004
2322 156 11003	RES 10K 1% 0W6 MTLFLM	1.0 EA	R005
2322 156 11002	RES 1K 1% 0W6 MTLFLM	2.0 EA	R006 R007
2100 116 23832	RES 3K83 1% 0.5W MTLFLM	1.0 EA	R008
9331 976 10112	TRANS BC547	1.0 EA	V001
9336 508 70682	TRANS BS170 (TO-92)	2.0 EA	V002 V003
9331 178 50112	DIODE BZX79C18	1.0 EA	V004
9333 341 80112	DIODE BAX12A	1.0 EA	V005

Table 3-8. CASE (VIDEO PROCESSOR) - 3913 467 05400

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 465 53400	EXTRUSION - TOP	1.0 EA	001
3913 465 53380	EXTRUSION - BOTTOM	1.0 EA	002
3913 464 06070	LABEL STRIP - (VIDEO PROCESSOR	1.0 EA	003
3913 464 09030	COVER SIDE (BLANK)	1.0 EA	007
3913 464 17980	COVER SIDE	1.0 EA	004
3913 464 08940	PANEL - FRONT	1.0 EA	005
3913 464 08990	PANEL - REAR	1.0 EA	006
3913 464 09010	CLIP - BOARD MOUNTING	6.0 EA	008
2500 708 98002	NUT No:4 ANGLE “SPIRE”	4.0 EA	009
3913 464 05120	CLIP RETAINING	2.0 EA	010
3913 463 20860	COVER	1.0 EA	011
3913 463 20780	MNTG BRKT	1.0 EA	012
2522 187 02046	SCR CSKSL ST ZN M2.5X10	8.0 EA	016
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	4.0 EA	125
@PN = 302 0632 000	**SCR CSK PHIL 10-32 X 5/8 SST**	**1.0 EA**	
2522 163 01005	SCR PNPZ ZN S/T-B 4X1/4	7.0 EA	020
2513 712 02007	WSH CRKL ST 18-8 M6	1.0 EA	022
2513 712 02004	WSH CRKL ST 18-8 M3	6.0 EA	023
357 0104 000	SPACER, 10-32 X 0.625 LG	1.0 PC	
2522 401 50008	NUT FULL HEX ST 18-8 M3	2.0 EA	026
2513 621 98164	EYELET 2.29MM O/D X 3.18*	5.0 EA	028
2522 177 04019	SCR PNSL ST ZN M2X6	4.0 EA	029
2512 795 02005	WSH SCHNR STNI M2.3	4.0 EA	030
2522 401 60005	NUT FULL HEX ST 18-8 M2	4.0 EA	031

Table 3-9. GRP DLY 2-45.75MHZ SYS M/N - 3913 466 2483006

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 2483000	GRP DLY CORR	1.0 EA	0010
3913 466 7149006	GRP DEL 2-45MHZ SYS M/N	1.0 EA	0015

Table 3-10. GRP DLY CORR - 3913 466 2483000

HARRIS P/N	DESCRIPTION	QTY/UM	REF. SYMBOLS/EXPLANATIONS
3913 467 05410	CASE (GROUP DELAY)	1.0 EA	003
2422 034 16776	CONTACT SKT 22-20 AWG	3.0 EA	016
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	6.0 EA	022
2413 015 01384	TAG SOLDER 2BA	2.0 PK	023
9390 253 60765	LED MTG KIT SIZE T1 3/4	1.0 EA	032
3913 081 66620	MOD RECORD PLATE 1 TO 12	1.0 EA	035 SLVE PTFE 0.89MM WHI TE 0813 105 03242 AS REQ WIRE EQU 0.5MM2 WHT 0722 239 03003 AS RE QD WIRE SN CU 0.8MM DIA 0313 051 01105 AS R EQD
9332 897 10682	LED 5MM HLMP-3507 GRN	1.0 EA	H001
2432 020 00234	PLUG RF SMB 50R B/H SLDR	2.0 EA	X001 X004
2422 025 02804	SKT 12 WAY (QIKMATE)	1.0 EA	X005
1913 000 10354	SLEEVE RUBBER 1.5X20 BLK	2.0 EA	038

Table 3-11. GRP DEL 2-45MHZ SYS M/N - 3913 466 7149006

HARRIS P/N	DESCRIPTION	QTY/UM	REF. SYMBOLS/EXPLANATIONS
3913 466 7149000	PCB ASSY GRP DELAY CORRECTOR	1.0 EA	0015
3913 469 50350	COIL 0.13-0.185UH	3.0 EA	L001:L004:L007
3913 469 50380	COIL 0.12-0.165UH	3.0 EA	L010:L013:L016
2322 156 11002	RES 1K 1% 0W6 MTLFLM	5.0 EA	AOT COMPONENT R006:R021:R036:R051: R066
2322 156 11502	RES 1K5 1% 0W6 MTLFLM	1.0 EA	AOT COMPONENT R081
2222 682 34101	CAP 100P 2% 100V N150 0.1"	2.0 EA	C064 C004

Table 3-12. PCB ASSY GRP DELAY CORRECTOR - 3913 466 7149000

HARRIS P/N	DESCRIPTION	QTY/UM	REF. SYMBOLS/EXPLANATIONS
3913 461 71490	PCB - GROUP DELAY	1.0 EA	001
2400 545 10026	BEAD FXD 3.5X1.2X3MM F14	6.0 EA	002
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	22.0 EA	WIRE SN CU 0.8MM DIA 0313 051 01105 AS R EQD
2413 535 00708	CHOKE 100UH 0W33 BS9751-N001-B	2.0 EA	L20:L21
2000 002 04681	CAP 680U 25V ELEC AX 85deg	2.0 EA	C83:C84
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	36.0 EA	008
2013 554 04043	CAP 4N7 -20%+80% 500V CER	44.0 EA	C001:C002:C003:C005:C009:C011:C012: C013:C014:C015:C017:C0 21:C023:C024: C025:C026:C027:C029:C033:C035:C036: C037:C 038:C039:C041:C045:C047:C048: C049:C050:C051:C053:C057:C05 9:C060: C061:C062:C063:C065:C069:C072:C073: C074:C081
2222 682 34101	CAP 100P 2% 100V N150 0.1"	4.0 EA	C016 C028 C040 C052
2222 809 09003	CAP 2P0 - 18P TRIM (18E)	6.0 EA	C006 C018 C030 C042 C054 C066
2222 682 09688	CAP 6P8 0.25PF 100V NPO 0.1"	6.0 EA	C007 C019 C031 C043 C055 C067
@PN = 2222 682 09188	**CAP 1P8 0.25PF 100V NPO 0.1"**	**5.0 EA**	C008 C020 C032 C044 C056
2222 682 34229	CAP 22P 2% 100V N150 0.1"	5.0 EA	C010 C022 C034 C046 C058
2222 682 34399	CAP 39P 2% 100V N150 0.1"	1.0 EA	C070
2222 682 34339	CAP 33P 2% 100V N150 0.1"	6.0 EA	C075 C076 C077 C078 C079 C080
2000 010 08159	CAP 15U 63V ELEC RAD PCB	1.0 EA	C082
3913 469 40180	COIL	5.0 EA	L002 L005 L008 L011 L014
3913 469 40010	CHOKE RF (1 HOLE FORMER)	7.0 EA	L003 L006 L009 L012 L015 L018 L019
2322 156 11001	RES 100R 1% 0W6 MTLFLM	12.0 EA	

			R001:R008:R016:R023:R031:R038:R046: R053 R061:R068:R076:R083
2122 362 00153	POT 100R 10% LIN W5 TOP ADJ	6.0 EA	R002 R017 R032 R047 R062 R077
2322 156 12201	RES 220R 1% 0W6 MTLFLM	6.0 EA	R003 R018 R033 R048 R063 R078
2322 156 13309	RES 33R 1% 0W6 MTLFLM	6.0 EA	R004 R019 R034 R049 R064 R079
2322 156 16801	RES 680R 1% 0W6 MTLFLM	6.0 EA	R005 R020 R035
2322 156 16801	RES 680R 1% 0W6 MTLFLM	6.0 EA	R050 R065 R080
2122 362 00154	POT 200R 10% LIN W5 TOP ADJ	6.0 EA	R007 R022 R037 R052 R067 R082
2322 156 14709	RES 47R 1% 0W6 MTLFLM	17.0 EA	R009 R013 R015 R024 R028 R030 R039 R043 R045 R054 R058 R060 R069 R073 R075 R088 R090
2322 156 11202	RES 1K2 1% 0W6 MTLFLM	7.0 EA	R010 R025 R040 R055 R070 R085 R094
2322 156 14301	RES 430R 1% 0W6 MTLFLM	6.0 EA	R011 R026 R041 R056 R071 R086
2322 156 11802	RES 1K8 1% 0W6 MTLFLM	6.0 EA	R012 R027 R042 R057 R072 R087
2322 156 14701	RES 470R 1% 0W6 MTLFLM	7.0 EA	R014 R029 R044 R059 R074 R089 R091
2322 156 11003	RES 10K 1% 0W6 MTLFLM	1.0 EA	R092
2322 156 11004	RES 100K 1% 0W6 MTLFLM	1.0 EA	R093
3913 469 40020	TRANSFORMER	6.0 EA	T001 T002 T003 T004 T005 T006
9330 765 30112	TRANS BFX89	12.0 EA	
@RD = V001 V002 V004 V005 V007 V008 V010 V011 V013 V014 V016 V017			
9330 295 71112	TRANS 2N2369A	6.0 EA	V003 V006 V009 V012V015 V018
9331 662 80765	DIODE 5082-2800	2.0 EA	V019:V020
9331 977 10112	TRANS BC557	1.0 EA	V021
9331 976 10112	TRANS BC547	1.0 EA	V022

Table 3-13. CASE (GROUP DELAY) - 3913 467 05410

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 465 53400	EXTRUSION - TOP	1.0 EA	001
3913 465 53380	EXTRUSION - BOTTOM	1.0 EA	002
3913 464 06080	LABEL STRIP - (GROUP DELAY)	1.0 EA	003
3913 464 09080	COVER SIDE	1.0 EA	004
3913 464 08920	PANEL - FRONT	1.0 EA	005
3913 464 09000	PANEL - REAR	1.0 EA	006
3913 464 09030	COVER SIDE (BLANK)	1.0 EA	007
3913 464 09010	CLIP - BOARD MOUNTING	6.0 EA	008
2500 708 98002	NUT No:4 ANGLE “SPIRE”	4.0 EA	009
3913 464 05120	CLIP RETAINING	2.0 EA	010
3913 463 20860	COVER	1.0 EA	011
3913 463 20780	MNTG BRKT	1.0 EA	012
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	4.0 EA	125
2522 187 02046	SCR CSKSL ST ZN M2.5X10	8.0 EA	016
302 0632 000	SCR CSK PHIL 10-32 X 5/8 SST	1.0 EA	
2522 163 01005	SCR PNPZ ZN S/T-B 4X1/4	7.0 EA	020
2513 712 02007	WSH CRKL ST 18-8 M6	1.0 EA	022
2513 712 02004	WSH CRKL ST 18-8 M3	6.0 EA	023
357 0104 000	SPACER, 10-32 X 0.625 LG	1.0 PC	
2522 401 50008	NUT FULL HEX ST 18-8 M3	8.0 EA	026
@PN = 2513 621 98164	**EYELET 2.29MM O/D X 3.18***	**5.0 EA**	028
2522 177 04019	SCR PNSL ST ZN M2X6	4.0 EA	029
2512 795 02005	WSH SCHNR STNI M2.3	4.0 EA	030
2522 401 60005	NUT FULL HEX ST 18-8 M2	4.0 EA	031

Table 3-14. COMBLINE FILTER BND4 - 3913 467 14710

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 47230	SOCKET ASSY	2.0 EA	001

3913 463 20310	TUNING SCREW	4.0 EA	003
3913 463 20320	CAPACITOR PLATE	8.0 EA	004
3913 463 20330	TUNING ROD (L)	4.0 EA	005
3913 463 20350	COVER PLATE (L)	2.0 EA	006
3913 463 20370	END PLATE (L)	2.0 EA	007
3913 463 20390	TOP PLATE (L)	1.0 EA	008
3913 463 20410	BOTTOM PLATE (L)	1.0 EA	009
3913 081 66620	MOD RECORD PLATE 1 TO 12	1.0 EA	010
2522 178 16059	SCR PNPZ ST NI M3 X 8	44.0 EA	012
2522 178 16062	SCR PNPZ ST NI M3 X 12	4.0 EA	013
2522 178 16083	SCR PNPZ ST NI M4 X 12	4.0 EA	014
2522 179 13094	SCR CSKPZ STNI M3 X 8	8.0 EA	016
2522 006 01006	SCR SKT CAP ST ZN M3X12	8.0 EA	018
2513 712 02004	WSH CRKL ST 18-8 M3	56.0 EA	020
2513 712 02005	WSH CRKL ST 18-8 M4	4.0 EA	021
2522 600 79017	WSH PLN FRM A ST 18-8 M3	8.0 EA	023
3913 081 60940	TYPE PLATE	1.0 EA	025 F.I.TO SUB-CONR.

Table 3-15. COMBLINE FILTER BND5 - 3913 467 14720

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 47230	SOCKET ASSY	2.0 EA	001
@PN = 3913 463 20310	**TUNING SCREW**	**4.0 EA**	003
3913 463 20320	CAPACITOR PLATE	8.0 EA	004
3913 463 20340	TUNING ROD (U)	4.0 EA	005
3913 463 20360	COVER PLATE (U)	2.0 EA	006
3913 463 20380	END PLATE (U)	2.0 EA	007
3913 463 20400	TOP PLATE (U)	1.0 EA	008
3913 463 20420	BOTTOM PLATE (U)	1.0 EA	009
3913 081 66620	MOD RECORD PLATE 1 TO 12	1.0 EA	010
2522 178 16059	SCR PNPZ ST NI M3 X 8	40.0 EA	012
2522 178 16062	SCR PNPZ ST NI M3 X 12	4.0 EA	013
2522 178 16083	SCR PNPZ ST NI M4 X 12	4.0 EA	014
2522 179 13094	SCR CSKPZ STNI M3 X 8	8.0 EA	016
2522 006 01006	SCR SKT CAP ST ZN M3X12	8.0 EA	018
2513 712 02004	WSH CRKL ST 18-8 M3	52.0 EA	020
2513 712 02005	WSH CRKL ST 18-8 M4	4.0 EA	021
2522 600 79017	WSH PLN FRM A ST 18-8 M3	8.0 EA	023
3913 081 60940	TYPE PLATE	1.0 EA	025 F.I.TO SUB-CONR.

Table 3-16. MOD/VSB ASSY SYS M - 992 9413 001

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
817 2336 213	TEST SPEC MOD & VSB	0.0 EA	
817 2336 214	TECH DATA MOD & VSB	0.0 EA	
992 9412 001	MOD/VSB FILTER SYS M PCB ASSY	1.0 EA	
939 8121 558	CASE ASSY MOD & VSB LIN CORR	1.0 EA	
2422 034 16776	CONTACT SKT 22-20 AWG	5.0 EA	
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	6.0 EA	
2413 015 01384	TAG SOLDER 2BA	5.0 PK	
@PN = 2432 020 00234	**PLUG RF SMB 50R B/H SLDR**	**5.0 EA**	X001:X002:X003:X004: X007
2422 025 02804	SKT 12 WAY (QIKMATE)	1.0 EA	X005
9332 897 10682	LED 5MM HLMP-3507 GRN	1.0 EA	H001
9390 253 60765	LED MTG KIT SIZE T1 3/4	1.0 EA	

Table 3-17. MOD/VSB FILTER SYS M PCB ASSY - 992 9412 001

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
839 8121 555	SCHEM MOD & VSB LIN CORR	0.0 EA	
843 5469 521	ASSY DWG MOD & VSB LIN CORR	0.0 EA	
843 5469 021	PCB MOD & VSB LIN CORR	1.0 EA	
2722 162 90771	MIXER DOUBLE BALANCED CM1	1.0 EA	A001
9336 772 00682	IC SL560CDP (DIL-8)	2.0 EA	A002:A003
2700 171 18009	FILTER SAW (SYSTEM-M/N)	1.0 EA	A004
9332 247 50749	IC LM741CN (DIL-8)	1.0 EA	A005
9337 497 30682	IC LM337LZ	1.0 EA	A006
9338 827 75682	IC LT1229CN8 (DIL-8)	1.0 EA	A007
3913 935 00038	REG 78L05 +5V 0.1A TO92	1.0 EA	A008
2222 630 19472	CAP 4N7 10% 100V MED-K 0.2"	29.0 EA	C001:C002:C003:C004:C005:C006:C009: C010:C011:C012:C013:C0 17:C018:C019: C020:C021:C022:C023:C024:C027:C028: C038:C 039:C040:C046:C047:C048:C049 C052
2222 683 34229	CAP 22P 2% 100V N150 0.2"	1.0 EA	C007
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	7.0 EA	C008:C032:C036:C043:C044: C045:C051
2222 122 56478	CAP 4U7 25V ELSOL	1.0 EA	C014
2222 122 55159	CAP 15U 16V ELSOL	5.0 EA	C015:C016:C025:C026: C034
2222 683 34689	CAP 68P 2% 100V N150 0.2"	1.0 EA	C029
2222 683 34121	CAP 120P 2% 100V N150 0.2"	1.0 EA	C035:C053:C054
@PN = 2012 310 03124	**CAP 330N 10% 63V PSTR 0.2" P**	**1.0 EA**	C037
2000 101 04688	CAP 6U8 16V ELSOL RAD/WIRE	2.0 EA	C041:C042
2222 683 09478	CAP 4P7 0.25PF 100V NPO 0.2"	1.0 EA	C050 (A.O.T.)
2012 310 03162	CAP 1U0 10% 50V PSTR 0.2" P	3.0 EA	C030:C031:C033
9336 774 30682	LED 3MM MV5774C RED	1.0 EA	H002
3913 469 50140	CHOKE RF (6 HOLE FORMER)	4.0 EA	L001:L002:L003:L004
3913 469 50570	COIL 28.3-31.5UH	1.0 EA	L005
2413 535 02011	CAN SCREENING ALUM	1.0 EA	FOR L005
2413 535 00501	CHOKE 0UH10 0W25 BS9751-N001-A	1.0 EA	L006
2413 535 00685	CHOKE 2UH2 0W25 BS9751-N0001-A	1.0 EA	L007
2322 156 15608	RES 5R6 1% 0W6 MTLFLM	1.0 EA	R013
2322 156 11009	RES 10R 1% 0W6 MTLFLM	3.0 EA	R010:R017:R081
2322 156 11209	RES 12R 1% 0W6 MTLFLM	1.0 EA	R004
2322 156 18208	RES 8R2 1% 0W6 MTLFLM	2.0 EA	R039:R040
2322 156 11809	RES 18R 1% 0W6 MTLFLM	1.0 EA	R071
2322 156 12209	RES 22R 1% 0W6 MTLFLM	3.0 EA	R007:R022:R024
2322 156 13309	RES 33R 1% 0W6 MTLFLM	1.0 EA	R045
2322 156 14709	RES 47R 1% 0W6 MTLFLM	3.0 EA	R031:R032 (AOT):R049
2322 156 15609	RES 56R 1% 0W6 MTLFLM	1.0 EA	R023
2322 156 16809	RES 68R 1% 0W6 MTLFLM	1.0 EA	R025
2322 156 17509	RES 75R 1% 0W6 MTLFLM	1.0 EA	R048
2322 156 18209	RES 82R 1% 0W6 MTLFLM	1.0 EA	R072
2322 156 19109	RES 91R 1% 0W6 MTLFLM	1.0 EA	R074
2322 156 11001	RES 100R 1% 0W6 MTLFLM	6.0 EA	R001:R003:R006:R009: R043:R018:R83
@PN = 2322 156 11201	**RES 120R 1% 0W6 MTLFLM**	**1.0 EA**	R059
2322 156 11501	RES 150R 1% 0W6 MTLFLM	5.0 EA	R008:R012:R030:R037: R069
2322 156 12201	RES 220R 1% 0W6 MTLFLM	3.0 EA	R015:R041:R056
2322 156 12401	RES 240R 1% 0W6 MTLFLM	1.0 EA	R073
2322 156 12701	RES 270R 1% 0W6 MTLFLM	1.0 EA	R052
2322 156 13901	RES 390R 1% 0W6 MTLFLM	3.0 EA	R044:R046:R082
2322 156 14701	RES 470R 1% 0W6 MTLFLM	5.0 EA	R011:R014:R057: R063:R079
2322 156 11002	RES 1K 1% 0W6 MTLFLM	8.0 EA	

			R002:R005:R047:R054:R060:R061:R062: R078 (AOT)
2322 156 11202	RES 1K2 1% 0W6 MTLFLM	1.0 EA	R016
2322 156 11502	RES 1K5 1% 0W6 MTLFLM	2.0 EA	R021:R070
2322 156 13902	RES 3K9 1% 0W6 MTLFLM	2.0 EA	R064:R068
2322 156 14702	RES 4K7 1% 0W6 MTLFLM	2.0 EA	R035:R036
2322 156 15602	RES 5K6 1% 0W6 MTLFLM	1.0 EA	R038
2322 156 11003	RES 10K 1% 0W6 MTLFLM	2.0 EA	R019:R020
2322 156 11203	RES 12K 1% 0W6 MTLFLM	1.0 EA	R033
2322 156 11803	RES 18K 1% 0W6 MTLFLM	1.0 EA	R055
2322 156 14703	RES 47K 1% 0W6 MTLFLM	1.0 EA	R067
2322 156 11004	RES 100K 1% 0W6 MTLFLM	2.0 EA	R034:R080
2322 156 14704	RES 470K 1% 0W6 MTLFLM	2.0 EA	R050:R051
2322 156 11005	RES 1M 1% 0W6 MTLFLM	1.0 EA	R077
2322 241 13225	RES 2M2 5% 0W25 MTLGLZ	1.0 EA	R058
2122 350 00645	POT 200R 10% LIN W5 SIDE ADJ	1.0 EA	R042
2122 362 00156	POT 1K0 10% LIN W5 TOP ADJ	1.0 EA	R053
2122 350 00515	POT 1K0 20% LIN W5	1.0 EA	R075
2122 362 00157	POT 2K0 10% LIN W5 TOP ADJ	1.0 EA	R065
2122 362 00158	POT 5K0 10% LIN W5 TOP ADJ	1.0 EA	
@RD = R076			
2122 362 00159	POT 10K 10% LIN W5 TOP ADJ	1.0 EA	R066
9331 177 60112	DIODE BZX79C7V5	2.0 EA	V001:V013
9331 662 80765	DIODE 5082-2800	2.0 EA	V002:V003
2407 137 00101	SWITCH THERMAL 75DEG S/STATE	1.0 EA	V004
9330 911 60112	TRANS BD135	1.0 EA	V005
9330 352 10112	TRANS 2N3866	2.0 EA	V006:V008
9330 219 20112	TRANS BSX20	3.0 EA	V007:V010:V012
9331 976 30112	TRANS BC547B	2.0 EA	V011:V020
380 0781 000	TRANS BS108	1.0 EA	V009
9331 977 10112	TRANS BC557	1.0 EA	V018
9330 473 10112	DIODE 1N916	4.0 EA	V014:V015:V016:V022:
9331 177 50112	DIODE BZX79C6V8	1.0 EA	V017
9337 293 80682	TRANS 2N5459	1.0 EA	V019
9333 341 80112	DIODE BAX12A	1.0 EA	V021
2413 015 02201	PIN TEST 1.3 X 1.02MM PCB	2.0 PK	TP1:TP2
2413 490 00001	SPACER TO5-001	2.0 EA	FOR V006:V008
3913 463 97400	HEATSINK	1.0 EA	
3913 463 97410	CLIP-SPRING	1.0 EA	
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	1.0 EA	
2522 178 15059	SCR PNPZ ST ZN M3 X 8	1.0 EA	
2513 712 02004	WSH CRKL ST 18-8 M3	1.0 EA	
2413 025 09503	PLUG SHORTING BLUE 0.200" PITC	2.0 EA	
2413 024 00425	SKT 1 WAY PCB 2.16MM DIA	6.0 EA	
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	17.0 EA	
@PN = 2413 015 14168	**TAG SOLDER PCB TAIL 2.5 X 0.9M**	**19.0 EA**	
2400 545 10026	BEAD FXD 3.5X1.2X3MM F14	1.0 EA	
3913 445 50120	HEADER 1 X 3	1.0 EA	LK03
2422 549 26002	SKT 2 WAY 2.54MM PITCH	1.0 EA	LK03
943 5396 223	FILTER INSULATING CARD	1.0 EA	
9390 289 00112	WASHER 56387A (TO-126) MICA	1.0 EA	
922 1206 283	HEAT RETAINING COVER	1.0 EA	
356 0252 000	CABLE TIE PLT1.5M-M	1.0 PM	

Table 3-18. CASE ASSY MOD & VSB LIN CORR - 939 8121 558

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 465 53400	EXTRUSION - TOP	1.0 EA	001
3913 465 53380	EXTRUSION - BOTTOM	1.0 EA	002
939 8121 557	LABEL STRIP(MOD & VSB LIN CORR	1.0 EA	003
3913 464 09030	COVER SIDE (BLANK)	1.0 EA	007
3913 464 17980	COVER SIDE	1.0 EA	004
3913 464 08920	PANEL - FRONT	1.0 EA	005
3913 464 09000	PANEL - REAR	1.0 EA	006
2500 708 98002	NUT No:4 ANGLE “SPIRE”	4.0 EA	009
3913 464 05120	CLIP RETAINING	2.0 EA	010
3913 463 20860	COVER	1.0 EA	011
3913 463 20780	MNTG BRKT	1.0 EA	012
2522 187 02046	SCR CSKSL ST ZN M2.5X10	8.0 EA	016
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	4.0 EA	125
302 0632 000	SCR CSK PHIL 10-32 X 5/8 SST	1.0 EA	
2522 163 01005	SCR PNPZ ZN S/T-B 4X1/4	7.0 EA	020
2513 712 02007	WSH CRKL ST 18-8 M6	1.0 EA	
@RD = 022			
2513 712 02004	WSH CRKL ST 18-8 M3	6.0 EA	023
357 0104 000	SPACER, 10-32 X 0.625 LG	1.0 PC	
2522 401 50008	NUT FULL HEX ST 18-8 M3	2.0 EA	026
2513 621 98164	EYELET 2.29MM O/D X 3.18*	5.0 EA	028
3913 464 19000	PLATE	1.0 EA	008
2522 177 04019	SCR PNSL ST ZN M2X6	4.0 EA	029
2512 795 02005	WSH SCHNR STNI M2.3	4.0 EA	030
2522 401 60005	NUT FULL HEX ST 18-8 M2	4.0 EA	031

Table 3-19. RX GRP DLY P1 CURVE - 3913 466 2481001

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 2481000	RX GROUP DELAY ASSY	1.0 EA	
3913 466 7096001	PCB - RX GROUP DELAY CURVE P1	1.0 EA	0040

Table 3-20. RX GROUP DELAY ASSY - 3913 466 2481000

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
335 0281 000	WASHER NYLON 5.08MM I/D	2.0 EA	FITTED TO X001:X004
2422 015 01002	SOLDERTAG M3 SNGL BR SN	1.0 EA	
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	1.0 EA	
3913 467 05390	CASE (RECEIVER GROUP DELAY)	1.0 EA	003
2522 401 50008	NUT FULL HEX ST 18-8 M3	1.0 EA	
2513 712 02004	WSH CRKL ST 18-8 M3	1.0 EA	
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	6.0 EA	018
2413 015 01384	TAG SOLDER 2BA	2.0 PK	029
620 2863 000	SKT RF SMB 50R B/HD INSUL	2.0 EA	X001:X004
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	1.0 EA	C001

Table 3-21. PCB - RX GROUP DELAY CURVE P1 - 3913 466 7096001

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
@PN = 3913 466 7096000	**PCB - RX GROUP DELAY**	**1.0 EA**	
2222 683 34479	CAP 47P 2% 100V N150 0.2"	1.0 EA	C001
2013 751 16404	CAP 390P 1% 350/400V MICA	5.0 EA	C002:C017:C019:C023 C025
2013 751 16406	CAP 470P 1% 350/400V MICA	1.0 EA	C003
2013 751 30046	CAP 2N7 1% 350/400V MICA	2.0 EA	C004:C005
2222 683 34279	CAP 27P 2% 100V N150 0.2"	1.0 EA	C006

2013 751 16402	CAP 330P 1% 350/400V MICA	1.0 EA	C007
2013 751 15583	CAP 1N8 1% 350/400V MICA	1.0 EA	C008
2222 683 34689	CAP 68P 2% 100V N150 0.2"	1.0 EA	C009
2013 751 16304	CAP 220P 1% 350/400V MICA	3.0 EA	C011:C013:C015
2222 683 34829	CAP 82P 2% 100V N150 0.2"	3.0 EA	C014:C016:C018
2222 683 34101	CAP 100P 2% 100V N150 0.2"	1.0 EA	C021
2222 683 34569	CAP 56P 2% 100V N150 0.2"	2.0 EA	C022:C024
3913 469 40290	COIL	1.0 EA	L001
3913 469 40250	COIL	1.0 EA	L002
3913 469 40280	COIL	2.0 EA	L003:L004
3913 469 40300	COIL	1.0 EA	L005
3913 469 40270	COIL	2.0 EA	L006:L008
3913 469 40260	COIL	1.0 EA	L007
3913 469 40240	COIL	1.0 EA	L009

Table 3-22. PCB - RX GROUP DELAY - 3913 466 7096000

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
@PN = 3913 461 70960	**PCB - RCVR GROUP DELAY**	**1.0 EA**	
			001
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	17.0 EA	002 WIRE SN CU 0.8MM DIA 0313 051 01105 AS R EQD

Table 3-23. CASE (RECEIVER GROUP DELAY) - 3913 467 05390

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 465 53400	EXTRUSION - TOP	1.0 EA	001
3913 465 53380	EXTRUSION - BOTTOM	1.0 EA	002
3913 464 06060	LABEL STRIP - (RECEIVER GROUP	1.0 EA	003
3913 464 09030	COVER SIDE (BLANK)	1.0 EA	007
3913 464 17980	COVER SIDE	1.0 EA	004
3913 464 22540	PANEL - FRONT	1.0 EA	005
3913 464 09000	PANEL - REAR	1.0 EA	006
3913 464 09010	CLIP - BOARD MOUNTING	6.0 EA	008
2500 708 98002	NUT No:4 ANGLE “SPIRE”	4.0 EA	009
3913 464 05120	CLIP RETAINING	2.0 EA	010
2522 187 02046	SCR CSKSL ST ZN M2.5X10	8.0 EA	016
302 0632 000	SCR CSK PHIL 10-32 X 5/8 SST	1.0 EA	
2522 163 01005	SCR PNPZ ZN S/T-B 4X1/4	5.0 EA	020
2513 712 02007	WSH CRKL ST 18-8 M6	1.0 EA	022
2513 712 02004	WSH CRKL ST 18-8 M3	4.0 EA	023
357 0104 000	SPACER, 10-32 X 0.625 LG	1.0 PC	
2513 621 98164	EYELET 2.29MM O/D X 3.18*	5.0 EA	028
2522 177 04019	SCR PNSL ST ZN M2X6	4.0 EA	029
2512 795 02005	WSH SCHNR STNI M2.3	4.0 EA	030
2522 401 60005	NUT FULL HEX ST 18-8 M2	4.0 EA	031

Table 3-24. DIFF.PHASE CORRECTOR ASSY - 3913 466 37970

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 75630	PCB ASSY- DIFF.PHASE CORR	1.0 EA	
@RD = 001			
3913 467 05250	CASE (DIFF PHASE CORRECTOR)	1.0 EA	002
2422 034 16776	CONTACT SKT 22-20 AWG	3.0 EA	025
2432 020 00234	PLUG RF SMB 50R B/H SLDR	4.0 EA	X001 X002 X003 X004
2422 025 02804	SKT 12 WAY (QIKMATE)	1.0 EA	X005
2413 015 01384	TAG SOLDER 2BA	4.0 PK	003
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	6.0 EA	

Table 3-25. PCB ASSY- DIFF.PHASE CORR - 3913 466 75630

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 461 75630	PCB - PHASE CORRECTOR	1.0 EA	001
3913 445 50470	HEADER 2 X 2	4.0 EA	010
3913 445 50120	HEADER 1 X 3	5.0 EA	011
2422 549 26016	SKT 2 WAY 2.54MM PITCH	9.0 EA	012
9332 912 10602	IC MC1496P	2.0 EA	0000
9336 772 00682	IC SL560CDP (DIL-8)	1.0 EA	A003
3913 935 00038	REG 78L05 +5V 0.1A TO92	1.0 EA	A004
3913 935 00039	REG 79L05 -5V 0.1A TO92	1.0 EA	A005
2000 101 04159	CAP 15U 16V ELSOL RAD/WIRE	4.0 EA	C001:C002:C044:C045
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	17.0 EA	C003:C004:C005:C006:C008:C009:C011: C013:C014:C016:C017:C0 18:C024:C025: C027:C028 C036
2222 683 34479	CAP 47P 2% 100V N150 0.2"	2.0 EA	C007 C015
2222 683 09478	CAP 4P7 0.25PF 100V NPO 0.2"	2.0 EA	C010 C023
2222 683 34101	CAP 100P 2% 100V N150 0.2"	1.0 EA	C012
2222 809 08003	CAP 5P0 - 57P TRIM (57E)	2.0 EA	C020 C030
@PN = 2222 683 34829	**CAP 82P 2% 100V N150 0.2"**	**1.0 EA**	C021
2000 300 00006	CAP 1N5 5% 100V PCRB RAD	2.0 EA	C022 C046
2222 683 09188	CAP 1P8 0.25PF 100V NPO 0.2"	1.0 EA	C026
2222 683 34689	CAP 68P 2% 100V N150 0.2"	1.0 EA	C031
2222 630 19471	CAP 470P 10% 100V MED-K 0.2"	2.0 EA	C032 C035
2222 630 19472	CAP 4N7 10% 100V MED-K 0.2"	9.0 EA	C033 C034 C037 C038 C039 C040 C041 C042 C043
2222 683 34399	CAP 39P 2% 100V N150 0.2"	1.0 EA	C047
3913 076 50110	DELAY LINE 315NS 5 TAPS	1.0 EA	D001
3913 469 50140	CHOKE RF (6 HOLE FORMER)	2.0 EA	L001 L002
2413 535 00124	CHOKE 1UH 0W33 BS9751-N0001-B	12.0 EA	L003 L004 L005 L006L007 L008 L009 L010 L011 L012 L013 L014
2413 535 00416	CHOKE 10UH 0W33 BS9751-N0001-C	2.0 EA	L015 L017
3913 469 40010	CHOKE RF (1 HOLE FORMER)	1.0 EA	L016
2322 156 17509	RES 75R 1% 0W6 MTLFLM	6.0 EA	R001 R064 R065 R067 R076 R099
2322 156 11002	RES 1K 1% 0W6 MTLFLM	19.0 EA	R006 R013 R016 R024 R027 R032 R039 R042 R046 R048 R049 R058 R062 R063 R077 R080 R090 R094 R114
2322 156 14701	RES 470R 1% 0W6 MTLFLM	17.0 EA	R008 R009 R019 R034 R035 R043 R044 R056 R057 R066 R071 R078 R079 R088 R089 R095 R098
2322 156 12202	RES 2K2 1% 0W6 MTLFLM	4.0 EA	R007 R012 R033 R038
2122 350 00354	POT 1K0 20% LIN W5	11.0 EA	R010 R015 R036 R041 R045 R053 R060 R086 R101 R108 R115
2322 156 18201	RES 820R 1% 0W6 MTLFLM	2.0 EA	R011 R037
2322 156 13302	RES 3K3 1% 0W6 MTLFLM	3.0 EA	R014 R040 R050
2322 156 11801	RES 180R 1% 0W6 MTLFLM	3.0 EA	R017 R025 R069
@PN = 2322 156 11502	**RES 1K5 1% 0W6 MTLFLM**	**8.0 EA**	R018 R026 R052 R054 R068 R074 R109 R110
2322 156 16802	RES 6K8 1% 0W6 MTLFLM	3.0 EA	R020 R028 R072
2322 156 14702	RES 4K7 1% 0W6 MTLFLM	7.0 EA	R021 R029 R051 R055 R073 R085 R087
2322 156 12201	RES 220R 1% 0W6 MTLFLM	3.0 EA	R022 R030 R075
2322 156 19109	RES 91R 1% 0W6 MTLFLM	1.0 EA	R023
2122 350 00468	POT 200R 20% LIN W5	1.0 EA	R031
2322 156 15109	RES 51R 1% 0W6 MTLFLM	2.0 EA	R047 R096
2322 156 13301	RES 330R 1% 0W6 MTLFLM	3.0 EA	R059 R061 R116
2122 350 00357	POT 500R 20% LIN W5	1.0 EA	R070

2322 156 16209	RES 62R 1% 0W6 MTLFLM	1.0 EA	R081
2322 156 11202	RES 1K2 1% 0W6 MTLFLM	2.0 EA	R082 R083
2322 156 16201	RES 620R 1% 0W6 MTLFLM	2.0 EA	R084 R091
2122 350 00361	POT 10K 20% LIN W5	1.0 EA	R092
2322 156 11003	RES 10K 1% 0W6 MTLFLM	1.0 EA	R093
2322 156 18209	RES 82R 1% 0W6 MTLFLM	1.0 EA	R097 SOT COMP 82-470R
2322 156 14709	RES 47R 1% 0W6 MTLFLM	1.0 EA	R100
2322 156 11501	RES 150R 1% 0W6 MTLFLM	1.0 EA	R102
2322 156 12001	RES 200R 1% 0W6 MTLFLM	2.0 EA	R103 R106
2322 156 11509	RES 15R 1% 0W6 MTLFLM	1.0 EA	R104
2322 156 13901	RES 390R 1% 0W6 MTLFLM	1.0 EA	R105
2322 156 16809	RES 68R 1% 0W6 MTLFLM	1.0 EA	R107
2322 156 11001	RES 100R 1% 0W6 MTLFLM	1.0 EA	R113
3913 469 03210	TRANSFORMER - PHASE SHIFT	1.0 EA	T001
9331 977 10112	TRANS BC557	5.0 EA	V004 V005 V016 V017 V032
9331 976 10112	TRANS BC547	12.0 EA	V003 V006 V015 V018 V019 V020 V021 V022 V023 V034 V035 V038
9330 219 20112	TRANS BSX20	8.0 EA	V007 V008 V011 V012 V030 V031 V040 V041
9336 508 70682	TRANS BS170 (TO-92)	3.0 EA	
@RD = V010 V014 V033			
9334 607 30112	DIODE BB212	6.0 EA	V024 V025 V026 V027 V028 V029
9337 874 40682	DIODE ZC822B (10%)	1.0 EA	V039
9331 739 70702	TRANS MPS3640	2.0 EA	V009:V013:
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	8.0 EA	015
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	11.0 EA	0100
2322 156 14703	RES 47K 1% 0W6 MTLFLM	2.0 EA	R117 R118

Table 3-26. CASE (DIFF PHASE CORRECTOR) - 3913 467 05250

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 465 53400	EXTRUSION - TOP	1.0 EA	001
3913 465 53380	EXTRUSION - BOTTOM	1.0 EA	002
3913 464 05930	LABEL STRIP - (DIFF PHASE CORR	1.0 EA	003
3913 464 09060	COVER SIDE	1.0 EA	004
3913 464 08920	PANEL - FRONT	1.0 EA	005
3913 464 09000	PANEL - REAR	1.0 EA	006
3913 464 09030	COVER SIDE (BLANK)	1.0 EA	007
3913 464 09010	CLIP - BOARD MOUNTING	6.0 EA	008
2500 708 98002	NUT No:4 ANGLE “SPIRE”	4.0 EA	009
3913 464 05120	CLIP RETAINING	2.0 EA	010
3913 463 20860	COVER	1.0 EA	011
3913 463 20780	MNTG BRKT	1.0 EA	012
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	4.0 EA	125
2522 187 02046	SCR CSKSL ST ZN M2.5X10	8.0 EA	016
302 0632 000	SCR CSK PHIL 10-32 X 5/8 SST	1.0 EA	
2522 163 01005	SCR PNPZ ZN S/T-B 4X1/4	7.0 EA	020
2513 712 02007	WSH CRKL ST 18-8 M6	1.0 EA	022
2513 712 02004	WSH CRKL ST 18-8 M3	6.0 EA	
@RD = 023			
357 0104 000	SPACER, 10-32 X 0.625 LG	1.0 PC	
2522 401 50008	NUT FULL HEX ST 18-8 M3	2.0 EA	026
2513 621 98164	EYELET 2.29MM O/D X 3.18*	5.0 EA	028
2522 177 04019	SCR PNSL ST ZN M2X6	4.0 EA	029
2512 795 02005	WSH SCHNR STNI M2.3	4.0 EA	030
2522 401 60005	NUT FULL HEX ST 18-8 M2	4.0 EA	310

Table 3-27. AURAL/VISUAL CORRECTOR - 992 9737 021

HARRIS P/N	DESCRIPTION	QTY/UM	REF. SYMBOLS/EXPLANATIONS
843 5396 685	WIRING DIAG AURAL/VIS CORRCTR	0.0 EA	
939 8121 833	AURAL/VISUAL CORR PCB ASSY	1.0 EA	
939 8121 886	CASE ASSY A/V CORRECTOR	1.0 EA	
2432 020 00234	PLUG RF SMB 50R B/H SLDR	7.0 EA	X001:X002:X004:X006 X007:X008:X009
2422 025 02804	SKT 12 WAY (QIKMATE)	1.0 EA	X005
2422 034 16776	CONTACT SKT 22-20 AWG	9.0 EA	X5/1.2.3.4.5.6.7.8& 12
2413 015 01384	TAG SOLDER 2BA	7.0 PK	

Table 3-28. AURAL/VISUAL CORR PCB ASSY - 939 8121 833

HARRIS P/N	DESCRIPTION	QTY/UM	REF. SYMBOLS/EXPLANATIONS
843 5469 553	ASSY DWG PCB AUR/VIS CORRECTOR	1.0 EA	
843 5469 053	PCB AURAL+VISUAL CORRECTOR	1.0 EA	0010
3913 466 78270	FILTER PCB	1.0 EA	0012
9336 772 00682	IC SL560CDP (DIL-8)	1.0 EA	A001
382 1624 000	IC CA3127E	4.0 EA	A002:A003:A004:A010
3913 935 12067	IC 74HC4538 RTRG (DIL-16	2.0 EA	A005:A006
9338 827 75682	IC LT1229CN8 (DIL-8)	2.0 EA	A007:A011
9335 613 10682	IC RC4558P-00	2.0 EA	A009:A015
9335 266 50602	IC NE5532N DIL-8	1.0 EA	
@RD = A012			
3913 935 00038	REG 78L05 +5V 0.1A TO92	1.0 EA	A013
9338 827 60682	IC OP37GP (DIL-8)	1.0 EA	A014
9338 827 77682	LED 10 SEG BARGRAPH.GRN W/DRVR	2.0 EA	A016:A017
9338 827 78682	IC EL2082CN (DIL-8)	1.0 EA	A018
2222 630 19472	CAP 4N7 10% 100V MED-K 0.2"	53.0 EA	C001:C003:C005:C006:C008:C009:C010: C011:C013:C015:C016:C0 17:C019:C021: C022:C023:C025:C026:C027:C028:C029: C030:C 031:C033:C034:C035:C039:C040: C041:C042:C043:C044:C045:C063:C065: C066:C067:C068:C074:C0 75:C077:C079: C080:C088:C089:C090:C091:C092:C096: C099:C 107:C117: C118
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	25.0 EA	C002:C036:C038:C046:C047:C051:C052: C053:C055:C056:C057:C0 84:C085:C087: C100:C101:C102:C103:C104:C105:C106: C108: C109:C114 C115
2012 310 03124	CAP 330N 10% 63V PSTR 0.2" P	2.0 EA	C119:C121
2222 630 19471	CAP 470P 10% 100V MED-K 0.2"	1.0 EA	C004
2013 751 16406	CAP 470P 1% 350/400V MICA	1.0 EA	C054
2222 683 58331	CAP 330P 2% 100V N750 0.2"	3.0 EA	C049:C082:C098
2222 809 05002	CAP 1P8 - 10P TRIM (10E)	1.0 EA	C113
2222 683 34151	CAP 150P 2% 100V N150 0.2"	1.0 EA	C018
2222 683 34121	CAP 120P 2% 100V N150 0.2"	2.0 EA	C032:C076
2012 310 03126	CAP 10N 10% 63V PSTR 0.2" P	4.0 EA	C037:C060:C086:C112
2222 683 34101	CAP 100P 2% 100V N150 0.2"	2.0 EA	C048:C081
2222 683 09338	CAP 3P3 0.25PF 100V NPO 0.2"	1.0 EA	C050
@PN = 2222 683 10109	**CAP 10P 2% 100V NPO 0.2"**	**3.0 EA**	C083:C116:C120
2222 683 09688	CAP 6P8 0.25PF 100V NPO 0.2"	1.0 EA	C097
2222 683 34689	CAP 68P 2% 100V N150 0.2"	1.0 EA	C058
2013 751 15593	CAP 1N5 1% 350/400V MICA	1.0 EA	C059
2222 683 58181	CAP 180P 2% 100V N750 0.2"	1.0 EA	C061
2013 017 01545	CAP 47U 20% 16V TANT	1.0 EA	C062

2000 101 04159	CAP 15U 16V ELSOL RAD/WIRE	5.0 EA	C093:C094:C095:C110: C111
2422 533 00254	LED 550-2406 RED PCB	1.0 EA	H001
2422 533 00252	LED 550-2206 GRN PCB	2.0 EA	H002:H003
3913 469 40010	CHOKE RF (1 HOLE FORMER)	1.0 EA	L001
3913 469 03210	TRANSFORMER - PHASE SHIFT	1.0 EA	L002
3913 469 51050	COIL 157.0 - 171.0UH	1.0 EA	L020
3913 469 50140	CHOKE RF (6 HOLE FORMER)	2.0 EA	L021:L022
3913 469 50590	COIL 1.33-2.32UH	1.0 EA	L009
2413 535 00419	CHOKE 100UH 0W33 BS9751-N001-D	3.0 EA	L007:L010:L017
2413 535 00431	CHOKE 47UH 0W33 BS9751-N0001-C	2.0 EA	L008:L018
2413 535 00124	CHOKE 1UH 0W33 BS9751-N0001-B	1.0 EA	L019
3913 445 50120	HEADER 1 X 3	5.0 EA	LINK 1:LINK 2:LINK 3 LINK 4:LINK 5
2422 549 26002	SKT 2 WAY 2.54MM PITCH	5.0 EA	LINK 1:LINK 2:LINK 3 LINK 4:LINK 5
2322 156 15109	RES 51R 1% 0W6 MTLFLM	13.0 EA	R001:R013:R015:R026:R063:R067:R082: R128: R129:R144:R158:R159: R167
2322 156 14701	RES 470R 1% 0W6 MTLFLM	4.0 EA	R002:R075:R126:R138
@PN = 2322 156 17509	**RES 75R 1% 0W6 MTLFLM**	**1.0 EA**	R003
2322 156 14709	RES 47R 1% 0W6 MTLFLM	4.0 EA	R006:R040:R094:R141
2322 156 11501	RES 150R 1% 0W6 MTLFLM	2.0 EA	R007:R124
2322 156 12001	RES 200R 1% 0W6 MTLFLM	5.0 EA	R008:R009:R010:R034: R115
2322 156 12701	RES 270R 1% 0W6 MTLFLM	2.0 EA	R011:R113
2322 156 11002	RES 1K 1% 0W6 MTLFLM	26.0 EA	R012:R021:R022:R023:R027:R028:R029: R032:R042:R057:R061:R0 70:R100:R119: R123:R133:R152:R168:R169:R191:R192: R199:R200:R203: R205:R206
2322 156 12209	RES 22R 1% 0W6 MTLFLM	5.0 EA	R016:R210:R211:R212: R213
2322 156 12002	RES 2K 1% 0W6 MTLFLM	1.0 EA	R019
2322 156 11003	RES 10K 1% 0W6 MTLFLM	15.0 EA	R053:R073:R076:R077:R078:R101:R104: R120:R136:R139:R140:R1 49:R153:R194: R197
2322 156 13301	RES 330R 1% 0W6 MTLFLM	8.0 EA	R024:R025:R030:R031:R059:R062:R064: R161 A.O.T.
2322 156 15601	RES 560R 1% 0W6 MTLFLM	3.0 EA	R033:R114:R155
2322 156 14301	RES 430R 1% 0W6 MTLFLM	2.0 EA	R037:R056
2322 156 11001	RES 100R 1% 0W6 MTLFLM	4.0 EA	R038:R148:R193:R196
2322 156 12201	RES 220R 1% 0W6 MTLFLM	9.0 EA	R005:R039:R058:R066:R117:R121:R163: R165: R166
2322 156 11502	RES 1K5 1% 0W6 MTLFLM	3.0 EA	R079:R142:R207
2322 156 14702	RES 4K7 1% 0W6 MTLFLM	4.0 EA	R043:R050:R093:R201
2322 156 16801	RES 680R 1% 0W6 MTLFLM	1.0 EA	R044
2322 156 11009	RES 10R 1% 0W6 MTLFLM	12.0 EA	R045:R046:R047:R065:R081:R103:R116: R122: R145:R156:R157:R164
2322 156 14708	RES 4R7 1% 0W6 MTLFLM	1.0 EA	R125
2322 156 13309	RES 33R 1% 0W6 MTLFLM	2.0 EA	R048:R060:
2322 156 13902	RES 3K9 1% 0W6 MTLFLM	1.0 EA	R020
2322 156 11004	RES 100K 1% 0W6 MTLFLM	3.0 EA	R052:R092:R102
2322 156 11005	RES 1M 1% 0W6 MTLFLM	2.0 EA	R055:R150
2322 156 17501	RES 750R 1% 0W6 MTLFLM	8.0 EA	R068:R069:R071:R072:R131:R132:R134: R135:
2322 156 15101	RES 510R 1% 0W6 MTLFLM	3.0 EA	
@RD = R080:R105:R143			
2322 156 14303	RES 43K 1% 0W6 MTLFLM	1.0 EA	R086
2322 156 15602	RES 5K6 1% 0W6 MTLFLM	1.0 EA	R089
2322 156 16802	RES 6K8 1% 0W6 MTLFLM	1.0 EA	R091
2322 156 13901	RES 390R 1% 0W6 MTLFLM	2.0 EA	R084:R107
2322 156 16809	RES 68R 1% 0W6 MTLFLM	1.0 EA	R014

2322 156 15609	RES 56R 1% 0W6 MTLFLM	1.0 EA	R036
2322 156 12202	RES 2K2 1% 0W6 MTLFLM	1.0 EA	R106
2322 156 19102	RES 9K1 1% 0W6 MTLFLM	1.0 EA	R095
2322 156 18201	RES 820R 1% 0W6 MTLFLM	1.0 EA	R083
2322 156 11801	RES 180R 1% 0W6 MTLFLM	2.0 EA	R127:R130
2322 156 11201	RES 120R 1% 0W6 MTLFLM	1.0 EA	0000 R160
2322 156 13602	RES 3K6 1% 0W6 MTLFLM	2.0 EA	R195:R198
2122 362 00156	POT 1K0 10% LIN W5 TOP ADJ	6.0 EA	R004:R017:R018:R054: R204:R209
2100 358 00011	POT 10R 10% OW5 1/4" DIA PCB	2.0 EA	R215:R216
2122 362 00153	POT 100R 10% LIN W5 TOP ADJ	3.0 EA	R035:R041:R154:
2100 358 00001	POT 100R 10% 0W5 1/4" DIA PCB	1.0 EA	R217
2122 362 00158	POT 5K0 10% LIN W5 TOP ADJ	2.0 EA	R074:R137
2122 362 00147	POT 20K 10% LIN W5 TOP ADJ	1.0 EA	R087
2122 362 00159	POT 10K 10% LIN W5 TOP ADJ	3.0 EA	R118:R151:R208
2400 125 00016	SWITCH TOG SPDT 0.1A (VERT PCB	2.0 EA	S001:S002
2400 125 00017	SWITCH TOG DPDT 0.1A (R/ANGL)	1.0 EA	S003
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	23.0 EA	
@PN = 2413 015 14168	**TAG SOLDER PCB TAIL 2.5 X 0.9M**	**18.0 EA**	
2413 015 02201	PIN TEST 1.3 X 1.02MM PCB	14.0 PK	TP01:TP02:TP03:TP04:TP05:TP06:TP07: TP08: TP09:TP10:TP11:TP12: TP13:TP14
2413 024 00425	SKT 1 WAY PCB 2.16MM DIA	3.0 EA	
9337 874 40682	DIODE ZC822B (10%)	1.0 EA	V001
9330 219 20112	TRANS BSX20	13.0 EA	V002:V003:V004:V006:V007:V010:V014: V016: V029:V032:V034:V040: V041
9330 765 30112	TRANS BFX89	7.0 EA	V005:V008:V009:V011: V013:V030:V033
9334 357 00765	DIODE 5082-3379	2.0 EA	V012:V039
9336 508 70682	TRANS BS170 (TO-92)	4.0 EA	V025:V027:V042:V043
9331 177 30112	DIODE BZX79C5V6	2.0 EA	V017:V035
380 0781 000	TRANS BS108	2.0 EA	V044:V045
9331 976 10112	TRANS BC547	1.0 EA	V020
9330 473 10112	DIODE 1N916	5.0 EA	V019:V022:V028:V031: V038
9331 977 10112	TRANS BC557	1.0 EA	V021
9336 814 30112	TRANS BSD214 OR SD215DE	3.0 EA	V023:V024:V054
9336 508 80682	TRANS BS250 (TO-92)	1.0 EA	V026
2400 490 01567	SKT 18 WAY x 0.3" R/A HOR/MGT	2.0 EA	USE WITH A016/A017

Table 3-29. FILTER PCB - 3913 466 78270

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 461 78270	PCB FILTER	1.0 EA	0010
2000 501 03689	CAP 68P 5% 50V NPO CER 1206	1.0 EA	C069
2000 501 03181	CAP 180P 5% 50V NPO CER 1206	1.0 EA	C073
2000 501 03399	CAP 39P 5% 50V NPO CER 1206	1.0 EA	C070
2000 501 03221	CAP 220P 5% 50V NPO CER 1206	1.0 EA	C071
@PN = 2000 501 03279	**CAP 27P 5% 50V NPO CER 1206**	**1.0 EA**	C072
2000 501 03101	CAP 100P 5% 50V NPO CER 1206	1.0 EA	C078
2400 535 10005	INDUCTOR 270nH 10% SIZE 1008	1.0 EA	L011
2400 535 10006	INDUCTOR 470nH 10% SIZE 1008	1.0 EA	L012
2400 535 10007	INDUCTOR 620nH 10% SIZE 1008	1.0 EA	L013
2400 535 10014	INDUCTOR 0.1uH 10% SIZE 1210	1.0 EA	L014
2400 535 10008	INDUCTOR 68nH 10% SIZE 1008	1.0 EA	L015
2400 535 10009	INDUCTOR 150nH 10% SIZE 1008	1.0 EA	L016
2400 040 10056	PIN - EYELET MOUNT	3.0 EA	0075
2513 621 98476	EYELET 1.6MM O/D X 3.7MM BRSS	3.0 EA	0080

Table 3-30. CASE ASSY A/V CORRECTOR - 939 8121 886

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 465 53400	EXTRUSION - TOP	1.0 EA	0001
3913 465 53390	EXTRUSION(BOTTOM)	1.0 EA	0002
3913 464 09030	COVER SIDE (BLANK)	1.0 EA	0007
3913 464 08930	PANEL - FRONT	1.0 EA	0005
3913 464 09000	PANEL - REAR	1.0 EA	0006
2500 708 98002	NUT No:4 ANGLE “SPIRE”	4.0 EA	0009
3913 464 05120	CLIP RETAINING	2.0 EA	0010
3913 463 20860	COVER	1.0 EA	0011
3913 463 20780	MNTG BRKT	1.0 EA	0012
2522 187 02046	SCR CSKSL ST ZN M2.5X10	8.0 EA	0016
302 0632 000	SCR CSK PHIL 10-32 X 5/8 SST	1.0 EA	
2522 163 01005	SCR PNPZ ZN S/T-B 4X1/4	55.0 EA	
@RD = 0020			
2513 712 02007	WSH CRKL ST 18-8 M6	1.0 EA	0022
2513 712 02004	WSH CRKL ST 18-8 M3	6.0 EA	0023
357 0104 000	SPACER, 10-32 X 0.625 LG	1.0 PC	
2522 401 50008	NUT FULL HEX ST 18-8 M3	2.0 EA	0026
2522 177 04019	SCR PNSL ST ZN M2X6	4.0 EA	0029
2512 795 02005	WSH SCHNR STNI M2.3	4.0 EA	0030
2522 401 60005	NUT FULL HEX ST 18-8 M2	4.0 EA	0031
943 5396 688	SIDE COVER	1.0 EA	
3913 464 20000	LABEL STRIP	1.0 EA	0003
3913 464 19000	PLATE	1.0 EA	
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	4.0 EA	125

Table 3-31. AURAL CORRECTOR ASSY - 992 9737 095

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
839 8121 919	SCHEM AURAL CORRECTOR	1.0 EA	
992 9502 051	AURAL CORRECTOR PCB ASSY	1.0 EA	
992 9737 094	CASE ASSY AURAL CORRECTOR	1.0 EA	
2422 025 02804	SKT 12 WAY (QIKMATE)	1.0 EA	
2422 034 16776	CONTACT SKT 22-20 AWG	4.0 EA	
2432 020 00234	PLUG RF SMB 50R B/H SLDR	2.0 EA	
0722 100 34005	CBL RF 50R RG178B/U TO MIL-C-1	0.50 RL	
2522 178 15059	SCR PNPZ ST 18-8 M3X8	1.0 EA	
2522 401 60008	NUT FULLHEX ST18-8 M3	1.0 EA	
2513 712 02004	WSH CRKL ST 18-8 M3	1.0 EA	
2522 600 17017	WSH PLN FRM A 18-8 M3	1.0 EA	
2422 015 01002	SOLDERTAG M3 SNGL BR SN	1.0 EA	
0313 051 01105	WIRE SN CU 0.8MM DIA	0.0 RL	USE AS REQUIRED

@T = AURAL CORRECTOR PCB ASSY - 992 9502 051

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
843 5469 088	PCB AURAL CORRECTOR	1.0 EA	
992 9502 052	VISION IP FILTER PCB ASSY	1.0 EA	
992 9502 053	CHROMINANCE FILTER PCB ASSY	1.0 EA	
383 0063 000	IC MAV-11SM	5.0 EA	A005:A009:A015: A019:A028
9340 000 30682	DIODE BAS16 (MARK-A6/A3	2.0 EA	V011:V012
9340 008 01682	TRANS SST215 (MARK-D5)	2.0 EA	V013:V014
9340 001 00682	TRANS BC857B (MARK-3F	1.0 EA	V009
9340 000 10682	TRANS BC847B (MARK-1F)	3.0 EA	V010:V026:V027
9340 000 80682	IC OP37GS (SO-8)	1.0 EA	A021
9340 001 50682	IC RC4558D (SO-8)	1.0 EA	A014
382 1624 000	IC CA3127E	1.0 EA	A023
9340 000 40682	DIODE BZX84-C4V7 (MARK-Z1	1.0 EA	V017

3913 935 00001	REG 7805 +5V 1.5A TO-220	1.0 EA	A011
3913 935 00039	REG 79L05 -5V 0.1A TO92	1.0 EA	A020
383 0171 000	IC MAR-3SM	5.0 EA	A006:A017:A029:
383 0171 000	IC MAR-3SM	5.0 EA	A039:A040
3913 935 12112	IC 74HC4538 2X1 RTRG (SO-16	2.0 EA	A012:A013
382 1608 000	IC, ERA-5SM	2.0 EA	A016:A018
9340 006 50682	IC LT1229CS8 (SO-8	3.0 EA	A007:A008:A022
383 0170 000	IC, LRPS-2-1	5.0 EA	A024:A025:A026:A027: A034
383 0172 000	IC, LRPS-3-1	4.0 EA	A030:A031:A032:A033
478 0429 000	XFMR, RF MODEL T4-1 SMT	3.0 EA	T001:T002:T003
382 1644 000	LIMITER, PLS-1, .1-150MHZ	4.0 EA	A035:A036:A037:A038
2000 504 01568	CAP 5P6 0P5 50V NPO CER 0805	9.0 EA	C009:C010:C034:C036:C118:C119:C120: C122: C124
@PN = 2000 504 02688	**CAP 6P8 0P5 50V NPO CER 0805**	**2.0 EA**	C040:C042
2000 504 03109	CAP 10P 5% 50V NPO CER 0805	4.0 EA	C037:C039:C125:C127
2000 504 03129	CAP 12pF 5% 50V NPO CER 0805	1.0 EA	C041
2000 504 03339	CAP 33pF 5% 50V NPO CER 0805	6.0 EA	C035:C123:C168:C169: C170:C171
2000 504 03689	CAP 68pF 5% 50V NPO CER 0805	3.0 EA	C038:C066:C126
2000 504 03101	CAP 100pF 5% 50V NPO CER 0805	2.0 EA	C088:C177
2000 504 03181	CAP 180pF 5% 50V NPO CER 0805	1.0 EA	C070
2000 504 03471	CAP 470pF 5% 50V NPO CER 0805	1.0 EA	C068
2000 504 01102	CAP 1N 0P25 NPO CER 0805	4.0 EA	C011:C027:C156:C157
2000 504 12152	CAP 1N5 10B827R CER 0805	1.0 EA	C069
2000 504 12103	CAP 10N 10% 50V X7R CER 0805	51.0 EA	C001:C006:C008:C013:C018:C019:C024: C026:C028:C033:C048:C0 54:C055:C060: C061:C072:C073:C078:C079:C049:C101: C086:C 087:C092:C095:C103:C104:C105: C106:C107:C117:C128:C129:C13 0:C131: C132:C133:C134:C135:C136:C137:C158: C159:C161:C162:C164:C165:C166:C167: C175:C176
2000 504 12104	CAP 100N 20% 50V X7R CER 0805	69.0 EA	C002:C004:C005:C007:C014:C015:C017: C020:C021:C023:C025:C0 29:C030:C032: C044:C045:C046:C047:C062:C063:C064: C065:C 067:C071:C074:C075:C076:C077: C080:C089:C090:C091:C093:C09 4:C096: C098:C099:C100:C102:C108:C114:C115: C138:C140:C1 41:C142:C143:C144:C145: C147:C148:C149:C151:C152:C154:C155 : C003:C016:C022:C031:C081:C097:C139: C146:C150:C153:C16 0: C163:C174
518 0111 000	CAP, TRIM 4.5-20PF 50V SMT	1.0 EA	C043
2000 504 03189	CAP 18pF 5% 50V NPO CER 0805	2.0 EA	C012:C121
@PN = 2000 101 04159	**CAP 15U 16V ELSOL RAD/WIRE**	**2.0 EA**	C084:C085
496 0088 009	IND CHIP 0.033UH 0805 20%	2.0 EA	L004:L037
496 0088 018	IND CHIP 0.18UH 0805 10%	2.0 EA	L052:L053
496 0088 010	IND CHIP 0.039UH 0805 20%	2.0 EA	L014:L015
496 0088 011	IND CHIP 0.047UH 0805 20%	4.0 EA	L010:L011:L042:L043
2400 535 10015	INDUCTOR 10uH 10% SIZE 1210	25.0 EA	L001:L002:L003:L005:L006:L007:L008: L009:L018:L019:L026:L0 27:L028:L029: L036:L038:L039:L040:L041:L046:L047: L048:L 049 L050:L051
496 0088 014	IND CHIP 0.082UH 0805 10%	4.0 EA	L012:L013:L044:L045
2413 535 00419	CHOKE 100UH 0W33 BS9751-N001-D	1.0 EA	L022
3913 469 50140	CHOKE RF (6 HOLE FORMER)	2.0 EA	L024:L025

2100 702 99999	RES OR 0R JUMPER SIZE 0805	2.0 EA	R086:R087
2100 702 01398	RES 3R9 1% 0.10W SIZE 0805	4.0 EA	R016:R017:R188:R189
2100 702 01159	RES 15R 1% 0.10W SIZE 0805	1.0 EA	R052
2100 702 01189	RES 18R 1% 0.10W SIZE 0805	5.0 EA	R049:R125:R231:R243: R208
2100 702 01129	RES 12R 1% 0.10W SIZE 0805	2.0 EA	R151:R251
2100 702 01309	RES 30R 1% 0.10W SIZE 0805	3.0 EA	R046:R079:R205
2100 702 01519	RES 51R 1% 0.10W SIZE 0805	19.0 EA	R011:R012:R014:R019:R020:R038:R173: R088:R089:R105:R118:R119:R178:R190: R191: R192:R193:R194:R199
2100 702 01101	RES 100R 1% 0.10W SIZE 0805	2.0 EA	R090:R111
2100 702 01181	RES 180R 1% 0.10W SIZE 0805	6.0 EA	R045:R047:R077:R078: R206:R207
2100 702 01301	RES 300R 1% 0.10W SIZE 0805	10.0 EA	R048:R050:R130:R150:R203:R204:R244: R245: R229:R230
2100 702 01111	RES 110R 1% 0.10W SIZE 0805	2.0 EA	R114:R116
2100 702 01331	RES 330R 1% 0.10W SIZE 0805	9.0 EA	R002:R022:R028:R040: R142:R179:R182:R195: R200
2100 702 01629	RES 62R 1% 0.10W SIZE 0805	1.0 EA	R246
2100 702 01391	RES 390R 1% 0.10W SIZE 0805	1.0 EA	R093
2100 702 01431	RES 430R 1% 0.10W SIZE 0805	4.0 EA	R080:R169:R250:R252
2100 700 02471	RES 470R 2% 0.25W Size 1206	28.0 EA	R007:R008:R009:R010:R126:R127:R128: R129:R131:R132:R133:R1 34:R135:R136: R137:R138:R156:R157:R158:R159:R160: R161:R 162:R163: R221:R222:R223:R224
2100 702 01561	RES 560R 1% 0.10W SIZE 0805	25.0 EA	R001:R006:R015:R018:R021:R026:R027: R032:R039:R044:R139:R1 40:R186:R187: R212:R213:R214:R215:R216:R217:R218: R220:R 168:R253: R255
2100 702 01681	RES 680R 1% 0.10WC SIZE 0805	9.0 EA	R005:R025:R031:R043:R141:R209:R210: R211: R219
2100 702 01751	RES 750R 1% 0.10W SIZE 0805	4.0 EA	R100:R101:R103:R104
2100 700 02821	RES 820R 2% 0.25W SIZE 1206	20.0 EA	R033:R034:R035:R036:R152:R153:R154: R155:R225:R226:R227:R228:R232:R233: R234: R235:R236:R237:R238: R239
2100 702 01821	RES 820R 1% 0.10W SIZE 0805	7.0 EA	R051:R053:R054:R056: R092:R172:R242
2100 702 01102	RES 1K0 1% 0.10W SIZE 0805	13.0 EA	R061:R062:R063:R064:R065:R066:R067: R068: R091:R099:R122:R171 R247
2100 702 01162	RES 1K6 1% 0.10W SIZE 0805	18.0 EA	R003:R004:R023:R024:R029:R030:R041: R042:R081:R082:R180:R1 81:R183:R184: R196:R197: R201:R202
2100 702 01202	RES 2K0 1% 0.10W SIZE 0805	4.0 EA	
@RD = R013:R037:R185:R198			
2100 702 01222	RES 2K2 1% 0.10W SIZE 0805	7.0 EA	R069:R071:R073:R075: R108:R123:R124
2100 702 01332	RES 3K3 1% 0.10W SIZE 0805	5.0 EA	R070:R072:R074:R076: R113
2100 702 01472	RES 4K7 1% 0.10W SIZE 0805	2.0 EA	R098:R120
2100 702 01562	RES 5K6 1% 0.10W SIZE 0805	1.0 EA	R106
2100 702 01103	RES 10K 1% 0.10W SIZE 0805	8.0 EA	R102:R107:R112:R117:R164:R170:R248: R249
2100 702 01104	RES 100K 1% 0.10W SIZE 0805	1.0 EA	R097
2100 702 05105	RES 1M0 5% 0.10W SIZE 0805	1.0 EA	R110
2322 156 15102	RES 5K1 1% 0W6 MTLFLM	1.0 EA	R177:AOT
2322 156 15602	RES 5K6 1% 0W6 MTLFLM	1.0 EA	R095:AOT
2322 156 18202	RES 8K2 1% 0W6 MTLFLM	1.0 EA	R096:AOT
2322 156 14303	RES 43K 1% 0W6 MTLFLM	1.0 EA	R165: AOT
2122 362 00154	POT 200R 10% LIN W5 TOP ADJ	1.0 EA	R115
2122 362 00159	POT 10K 10% LIN W5 TOP ADJ	6.0 EA	R057:R058:R059:R060: R164:R166
2122 350 00459	POT 10K 10% LIN W5 SIDE ADJ	1.0 EA	R167
2122 362 00147	POT 20K 10% LIN W5 TOP ADJ	1.0 EA	R094

2100 401 00015	POT 100R 20% CER 4mm SQ S/M	2.0 EA	R055:R254
385 0017 000	DIODE HSMP3804 SOT23	18.0 EA	V001:V002:V003:V004:V005:V006:V007: V008:V015:V016:V018:V0 19:V020:V021: V022:V023: V024:V025
3913 445 50120	HEADER 1 X 3	5.0 EA	LK01:LK02:LK03:LK04: LK06
2422 549 26002	SKT 2 WAY 2.54MM PITCH	5.0 EA	LK01:LK02:LK03:LK04: LK06
2413 024 00425	SKT 1 WAY PCB 2.16MM DIA	9.0 EA	
@RD =			
2432 020 00191	PLUG RF SMB 50R PCB MGT	4.0 EA	X006:X007:X008:X011
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	8.0 EA	R095:R096:R165:R177
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	9.0 EA	
2400 125 00016	SWITCH TOG SPDT 0.1A (VERT PCB	1.0 EA	S001
2522 178 15059	SCR PNPZ ST 18-8 M3X8	1.0 EA	
2522 401 60008	NUT FULLHEX ST18-8 M3	1.0 EA	
2522 600 17017	WSH PLN FRM A 18-8 M3	1.0 EA	
2513 712 02004	WSH CRKL ST 18-8 M3	1.0 EA	

Table 3-32. CHROMINANCE FILTER PCB ASSY - 992 9502 053

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
843 5469 089	PCB VISION IP FILTER	1.0 EA	
2000 504 03271	CAP 270pF 5% 50V NPO CER 0805	1.0 EA	C006
518 0112 000	CAP, TRIM 2-10PF 50V SMT	2.0 EA	C001:C002
518 0111 000	CAP, TRIM 4.5-20PF 50V SMT	1.0 EA	C003
2400 535 10013	INDUCTOR 0.56UH 5% SIZE 1210	2.0 EA	L001:L002
496 0088 011	IND CHIP 0.047UH 0805 20%	1.0 EA	L003
2400 040 10056	PIN - EYELET MOUNT	3.0 EA	
2513 621 98476	EYELET 1.6MM O/D X 3.7MM BRSS	3.0 EA	
2000 504 03129	CAP 12pF 5% 50V NPO CER 0805	2.0 EA	C004:C005

Table 3-33. VISION IP FILTER PCB ASSY - 992 9502 052

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
843 5469 089	PCB VISION IP FILTER	1.0 EA	
2000 504 03121	CAP 120pF 5% 50V NPO CER 0805	2.0 EA	C006
518 0112 000	CAP, TRIM 2-10PF 50V SMT	2.0 EA	C001:C002
@PN = 518 0111 000	**CAP, TRIM 4.5-20PF 50V SMT**	**1.0 EA**	C003
2400 535 10002	INDUCTOR 2.2uH 5% SIZE 1210	2.0 EA	L001:L002
496 0088 014	IND CHIP 0.082uH 0805 10%	1.0 EA	L003
2400 040 10056	PIN - EYELET MOUNT	3.0 EA	
2513 621 98476	EYELET 1.6MM O/D X 3.7MM BRSS	3.0 EA	

Table 3-34. CASE ASSY AURAL CORRECTOR - 992 9737 094

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 465 53400	EXTRUSION - TOP	1.0 EA	001
3913 465 53380	EXTRUSION - BOTTOM	1.0 EA	002
922 1206 355	LABEL STRIP AURAL CORRECTOR	1.0 EA	003
3913 464 17980	COVER SIDE	1.0 EA	004
3913 464 21270	PANEL FRONT	1.0 EA	005
3913 464 08990	PANEL - REAR	1.0 EA	006
3913 464 09030	COVER SIDE (BLANK)	1.0 EA	007
2500 708 98002	NUT No:4 ANGLE “SPIRE”	4.0 EA	009
3913 464 05120	CLIP RETAINING	2.0 EA	010
3913 463 20860	COVER	1.0 EA	011
3913 463 20780	MNTG BRKT	1.0 EA	012
2522 187 02046	SCR CSKSL 18-8 M2.5X10	8.0 EA	016

302 0632 000	SCR CSK PHIL 10-32 X 5/8 SST	1.0 EA	
2522 163 01005	SCR PNPZ ZN S/T-B 4X1/4	7.0 EA	020
2513 712 02007	WSH CRKL ST 18-8 M6	1.0 EA	022
2513 712 02004	WSH CRKL ST 18-8 M3	6.0 EA	023
357 0104 000	SPACER, 10-32 X 0.625 LG	1.0 PC	
2522 401 50008	NUT FULLHEX ST18-8 M3	2.0 EA	026
2513 621 98164	EYELET 2.29MM O/D X 3.18*	5.0 EA	028
2522 177 04019	SCR PNSL ST18-8 M2X6	4.0 EA	
@RD = 029			
2512 795 02005	WSH SCHNR STNI M2.3	4.0 EA	030
2522 401 60005	NUT FULLHEX ST18-8 M2	4.0 EA	031

Table 3-35. COMBINED MIXER/UP CONVERTER - 3913 467 13260

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 461 77510	PCB - UP CONVERTER (SND/VIS MI	1.0 EA	
3913 088 00260	SCREENING CAN BASE 133 X 72MM	1.0 EA	
3913 088 00270	SCREENING CAN LID 132.8 X 72MM	1.0 EA	
3913 081 66620	MOD RECORD PLATE 1 TO 12	1.0 EA	
3913 461 25310	LABEL	1.0 EA	
2700 162 92013	MIXER - FREQUENCY 5 - 1000MHz	1.0 EA	A001
2000 501 03331	CAP 330P 5% 50V NPO CER 1206	16.0 EA	C001 C002 C003 C004 C005 C006 C007 C008 C014 C016 C017 C018 C019 C020 C021 C050
2000 501 11104	CAP 100N 10% 50V X7R CER 1206	5.0 EA	C009 C010 C011 C012 C043
2000 501 01109	CAP 10P 5% 50V NPO CER 1206	3.0 EA	CAP 10P 5% 50/63V C013 C044 C045
2000 501 01478	CAP 4P7 0P5 50V NPO CER 1206	1.0 EA	C015
2400 535 10014	INDUCTOR 0.1uH 10% SIZE 1210	2.0 EA	L001 L003
2100 700 05369	RES 36R 5% 0.25W Size 1206	3.0 EA	R004 R011
2100 700 05151	RES 150R 5% 0.25W Size 1206	8.0 EA	R002 R003 R005 R010 R025 R033 R027 R031
2100 700 05152	RES 1K5 5% 0.25W Size 1206	1.0 EA	R006
2100 700 05221	RES 220R 5% 0.25W Size 1206	1.0 EA	R007
2100 700 05222	RES 2K2 5% 0.25W Size 1206	4.0 EA	
@RD = R008 R014 R017 R026			
2100 700 05181	RES 180R 5% 0.25W Size 1206	4.0 EA	R009 R012 R019 R028
2100 700 05202	RES 2K 5% 0.25W Size 1206	4.0 EA	R013 R018 R024 R030
2100 700 05519	RES 51R 5% 0.25W Size 1206	3.0 EA	R015 R032 R034
2100 700 05109	RES 10R 5% 0.25W Size 1206	4.0 EA	R020 R036 R016 R073
2100 700 05569	RES 56R 5% 0.25W Size 1206	1.0 EA	R021
2100 700 05829	RES 82R 5% 0.25W Size 1206	1.0 EA	R022
2100 700 05911	RES 910R 5% 0.25W Size 1206	1.0 EA	R023
2100 700 05189	RES 18R 5% 0.25W Size 1206	1.0 EA	R029
2100 700 05101	RES 100R 5% 0.25W Size 1206	1.0 EA	R035
9340 000 00682	TRANS BFG197 (MARK-V5	5.0 EA	V001 V002 V003 V004 V005
2400 031 00011	SKT RF SMC 50R PCB MTG STRGHT	4.0 EA	X001 X002 X003 X004
2422 021 98239	HEADER 6 WAY 0.1" PITCH	1.0 EA	X009

Table 3-36. FLYWHEEL SYNC DELAY ASSY - 3913 467 12420

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 77810	PCB ASSY - FLYWHEEL SYNC DELAY	1.0 EA	010
3913 465 00450	CASE - DIGITAL SYNC DELAY	1.0 EA	020
3913 461 25320	LABEL	1.0 EA	030
3913 081 66620	MOD RECORD PLATE 1 TO 12	1.0 EA	040
2413 015 01144	TERM INSL F/THRO 3.96MM	2.0 EA	060
2422 015 01002	SOLDERTAG M3 SNGL BR SN	2.0 EA	070
2413 015 01384	TAG SOLDER 2BA	1.0 PK	075

@PN = 2522 401 50008	**NUT FULL HEX ST 18-8 M3**	**1.0 EA**	
			080
2522 600 79017	WSH PLN FRM A ST 18-8 M3	4.0 EA	085
2513 712 02004	WSH CRKL ST 18-8 M3	5.0 EA	090
2522 178 15059	SCR PNPZ ST ZN M3 X 8	5.0 EA	095 110
2432 020 00234	PLUG RF SMB 50R B/H SLDR	2.0 EA	X001 X002

Table 3-37. PCB ASSY - FLYWHEEL SYNC DELAY - 3913 466 77810

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 461 77810	PCB - FLYWHEEL SYNC DELAY	1.0 EA	010
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	20.0 EA	020
2422 487 89564	SPACER LED 5MM DIA X 15.9	1.0 EA	030
2432 490 00002	SKT DIL 14WAY x 0.3" FL/FRAME	1.0 EA	040
2432 490 00003	SKT DIL 16WAY x 0.3' FL/FRAME	4.0 EA	050
9333 243 30602	IC HEF4528BP	2.0 EA	A001 A004
9332 966 90602	IC HEF4046BP	1.0 EA	A002
9332 824 60602	IC HEF4520BP	1.0 EA	A003
9332 776 10602	IC HEF4013BP	1.0 EA	A005
2000 101 04109	CAP 10U 16V ELSOL RAD/WIRE	1.0 EA	C001
2013 751 15572	CAP 1N2 1% 350/400V MICA	1.0 EA	C002
2222 683 58181	CAP 180P 2% 100V N750 0.2"	1.0 EA	C003:S.O.T
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	6.0 EA	C004:C009:C010:C011 C012:C013
2013 751 15593	CAP 1N5 1% 350/400V MICA	1.0 EA	C006
2000 301 01104	CAP 100N 10% 100V PETP 10MM	1.0 EA	
@RD = C005			
2013 751 15223	CAP 750P 1% 350/400V MICA	1.0 EA	C007
2013 751 50834	CAP 1N1 1% 350/400V MICA	1.0 EA	C008
9332 897 20682	LED 5MM HLMP-3301 RED	1.0 EA	H001
2322 156 11009	RES 10R 1% 0W6 MTLFLM	1.0 EA	R015
2322 156 11003	RES 10K 1% 0W6 MTLFLM	3.0 EA	R004 R005 R014
2322 156 17509	RES 75R 1% 0W6 MTLFLM	2.0 EA	R002 R013
2322 156 11002	RES 1K 1% 0W6 MTLFLM	3.0 EA	R003 R006 R016
2322 156 14701	RES 470R 1% 0W6 MTLFLM	2.0 EA	R007 R008
2322 156 11004	RES 100K 1% 0W6 MTLFLM	2.0 EA	R001:S.O.T R009
2322 156 13301	RES 330R 1% 0W6 MTLFLM	1.0 EA	R012
2122 350 00361	POT 10K 20% LIN W5	2.0 EA	R010 R011
9336 508 80682	TRANS BS250 (TO-92)	1.0 EA	V001
9330 219 20112	TRANS BSX20	1.0 EA	V002
9330 473 10112	DIODE 1N916	2.0 EA	V003 V004
9331 976 10112	TRANS BC547	1.0 EA	V005

Table 3-38. CASE - DIGITAL SYNC DELAY - 3913 465 00450

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
2413 550 00002	BOX D/CAST 111X60X30MM	1.0 EA	001

Table 3-39. XSTAL OSC - 45.75MHz IF - 4313 466 4032402

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
4313 466 4032400	XSTAL OSC - NO CRYSTAL	1.0 EA	0010
3913 074 51050	CRYSTAL 45.75000MHZ	1.0 EA	B001
2013 751 07165	CAP 56P +-1pF 350/400V 0.2" P	1.0 EA	C001

Table 3-40. XSTAL OSC - CHANNEL - 4313 466 4032403

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
4313 466 4032400	XSTAL OSC - NO CRYSTAL	1.0 EA	0010
3913 074 51260	CRYSTAL.CHANNEL.TO SPEC	1.0 EA	B001

@PN = 2013 751 07154 CAP 47P +-1pF 350/400V 0.2" P 1.0 EA

			C001 FREQ 45-50MHz
2013 751 07163	CAP 27P +-1pF 350/400V 0.2" P	1.0 EA	C001 FREQ 55-65MHz
2013 751 07164	CAP 39P +-1pF 350/400V 0.2" P	1.0 EA	C001 FREQ 48-55MHz
2013 751 07165	CAP 56P +-1pF 350/400V 0.2" P	1.0 EA	C001 FREQ 42-46MHz

Table 3-41. XSTAL OSC - NO CRYSTAL - 4313 466 4032400

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 41320	XTAL OSCILLATOR CASE ASSY	1.0 EA	002
3913 081 66620	MOD RECORD PLATE 1 TO 12	1.0 EA	005
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	18.0 EA	006
2522 178 15062	SCR PNPZ ST 18-8 M3 X 12	5.0 EA	007
2522 401 50008	NUT FULL HEX ST 18-8 M3	2.0 EA	008
2513 712 02004	WSH CRKL ST 18-8 M3	9.0 EA	009
2422 015 01002	SOLDERTAG M3 SNGL BR SN	2.0 EA	010
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	1.0 EA	C023
2000 555 00001	CAP 1N 20% 500V CER F/T	4.0 EA	C019 C020 C021 C022
2113 253 02518	RES 1R0 1% 3W W/W	1.0 EA	R031
8213 268 79051	SKT RF TNC B/HEAD 50R	3.0 EA	X001 X002 X003
3913 466 72930	PCB ASSY - O/P MONITOR	1.0 EA	029
3913 461 40160	OVEN REG/OUTPUT AMP.PWB	1.0 EA	030
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	12.0 EA	008
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	17.0 EA	009
3913 463 42190	OVEN COVER PILLAR	2.0 EA	033
3913 463 42170	OVEN SUPPORT PILLAR	2.0 EA	034
@PN = 3913 463 42160 OVEN COVER 1.0 EA			
			035
2522 178 15059	SCR PNPZ ST ZN M3 X 8	2.0 EA	036
2522 600 79017	WSH PLN FRM A ST 18-8 M3	2.0 EA	037
9390 238 60112	WASHER 56326 (TO-126) LOAD	2.0 EA	043
3913 935 00057	REG 7808 +8V 1.5A (TO-220)	1.0 EA	A001
9332 247 50749	IC LM741CN (DIL-8)	1.0 EA	A002
2013 554 04043	CAP 4N7 -20%+80% 500V CER	8.0 EA	C010 C011 C012 C013 C014 C015 C016 C017
2000 301 01334	CAP 330N 10% 100V PETP 15MM	1.0 EA	C018
3913 469 40010	CHOKE RF (1 HOLE FORMER)	4.0 EA	L003 L005 L006 L007
2413 535 00333	CHOKE 3UH3 0W33 BS9751-N0001-C	1.0 EA	L004
2322 156 16801	RES 680R 1% 0W6 MTLFLM	1.0 EA	R011
2322 156 12001	RES 200R 1% 0W6 MTLFLM	4.0 EA	R012 R013 R015 R017
2322 156 11301	RES 130R 1% 0W6 MTLFLM	3.0 EA	R014 R016 R018
2122 362 00146	POT 10K 10% LIN W5	1.0 EA	R019
2322 156 15602	RES 5K6 1% 0W6 MTLFLM	1.0 EA	R020
2322 156 11802	RES 1K8 1% 0W6 MTLFLM	2.0 EA	0000 R021 R024
2122 362 00143	POT 1K0 10% LIN W5	1.0 EA	R022
2322 156 11302	RES 1K3 1% 0W6 MTLFLM	1.0 EA	R023
2322 626 22103	RES NTC 10K 10% 0W5	1.0 EA	R025
2322 156 15601	RES 560R 1% 0W6 MTLFLM	2.0 EA	R026 R027
2322 241 13105	RES 1M 5% 0W25 MTLGLZ	1.0 EA	R028 R029;DO NOT FIT-AOT: R030;DO NOT FIT-AOT:
3913 469 40020	TRANSFORMER	3.0 EA	T001 T002 T003
9330 295 71112	TRANS 2N2369A	3.0 EA	V004 V005 V006
9331 176 70112	DIODE BZX79C3V3	1.0 EA	V007
@PN = 9330 441 00112 TRANS BCY70 1.0 EA			
			V008
9330 822 50112	TRANS BD132	2.0 EA	V009 V010
9330 473 10112	DIODE 1N916	1.0 EA	V011
3913 463 42140	OVEN CASE	1.0 EA	070

3913 463 42150	OVEN CASE LTD	1.0 EA	071
3913 463 42180	PWB SUPPORT PILLAR	1.0 EA	072
3913 461 40150	PWB - OSCILLATOR	1.0 EA	C001 SELECT FROM P/N RANGE 2013 751 07153 TO 2013 751 07251
2022 801 00057	CAP TRIM 1P5-14P	2.0 EA	C002 C003
2013 751 07251	CAP 12P +-1pF 350/400V 0.2" P	1.0 EA	C004
2222 629 18472	CAP 4N7 -20+80 63V HI-K 0.1"	5.0 EA	C005:C006:C007:C008
2222 629 18472	CAP 4N7 -20+80 63V HI-K 0.1"	5.0 EA	C009
3913 469 40220	COIL	1.0 EA	L001
2413 535 00333	CHOKE 3UH3 0W33 BS9751-N0001-C	1.0 EA	L002
2322 156 12002	RES 2K 1% 0W6 MTLFLM	2.0 EA	R001 R007
2322 156 11002	RES 1K 1% 0W6 MTLFLM	2.0 EA	R002 R008
2322 156 11802	RES 1K8 1% 0W6 MTLFLM	1.0 EA	R003
2322 156 16801	RES 680R 1% 0W6 MTLFLM	1.0 EA	R004
2322 156 11004	RES 100K 1% 0W6 MTLFLM	2.0 EA	R005 R006
2322 156 11501	RES 150R 1% 0W6 MTLFLM	1.0 EA	R009
2322 156 11001	RES 100R 1% 0W6 MTLFLM	1.0 EA	R010
9330 295 71112	TRANS 2N2369A	2.0 EA	V001 V003
9337 743 20682	DIODE 1N5461A	1.0 EA	V002
2522 178 15129	SCR PNPZ ST 18-8 M6X10	1.0 EA	100
2522 401 50013	NUT FULL HEX ST 18-8 M6	1.0 EA	110
2513 712 02007	WSH CRKL ST 18-8 M6	1.0 EA	270
@PN = 3913 463 20670	**P.W.B. SUPPORT BRKT**	**1.0 EA**	280
9332 897 10682	LED 5MM HLMP-3507 GRN	1.0 EA	H001
9390 253 60765	LED MTG KIT SIZE T1 3/4	1.0 EA	330
2400 040 10032	WSH LOCK INT TOOTH 3/8" I/D	3.0 EA	340

Table 3-42. PCB ASSY - O/P MONITOR - 3913 466 72930

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 461 72930	PCB - O/P MONITOR	1.0 EA	001
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	3.0 EA	002
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	4.0 EA	003
0813 105 03242	SLVE PTFE 0.89MM WHITE	0.150 ME	004
9333 905 60749	IC LM348N (DIL-14	1.0 EA	A001
9333 241 90602	IC HEF4000BP	1.0 EA	A002
2013 554 04043	CAP 4N7 -20%+80% 500V CER	6.0 EA	C001 C002 C004 C005 C007 C008
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	3.0 EA	C003 C006 C009
2322 156 14701	RES 470R 1% 0W6 MTLFLM	3.0 EA	R001 R006 R011
2322 156 11003	RES 10K 1% 0W6 MTLFLM	10.0 EA	R002 R003 R005 R007 R008 R010 R012 R013 R015 R016
2322 156 13601	RES 360R 1% 0W6 MTLFLM	3.0 EA	R004 R009 R014
2322 156 11202	RES 1K2 1% 0W6 MTLFLM	1.0 EA	R017
9331 662 80765	DIODE 5082-2800	6.0 EA	V001 V002 V003 V004 V005 V006
9331 976 10112	TRANS BC547	1.0 EA	V007

Table 3-43. XTAL OSCILLATOR CASE ASSY - 3913 466 41320

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 463 42090	END PLATE - CAPACITOR MTG	1.0 EA	001
3913 463 42100	ENDPLATE - SOCKET MTG	1.0 EA	002
3913 463 42110	BOARD MTG BARS	2.0 EA	003
3913 463 42130	BASE PLATE	1.0 EA	
@RD = 004			
3913 463 42120	COVER	1.0 EA	005
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	16.0 EA	009
2522 178 15062	SCR PNPZ ST 18-8 M3 X 12	4.0 EA	010

2513 712 02004	WSH CRKL ST 18-8 M3	20.0 EA	018
2522 600 79017	WSH PLN FRM A ST 18-8 M3	4.0 EA	019

Table 3-44. HARMONIC GENERATOR - 3913 467 13220

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 466 78070	PCB ASSY HARMONIC GENERATOR	1.0 EA	010
3913 467 13230	CASE ASSY	1.0 EA	020
3913 465 01480	MODIFIED HEATSINK	1.0 EA	0030
3913 466 41060	MODIFIED BULKHEAD SOCKET	2.0 EA	X001 X002
3913 464 19330	DIODE MOUNT	1.0 EA	050
3913 463 31620	DIODE CLAMP SCREW	1.0 EA	060
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	12.0 EA	070
2513 712 02004	WSH CRKL ST 18-8 M3	10.0 EA	075
2400 040 10032	WSH LOCK INT TOOTH 3/8" I/D	2.0 EA	
2522 178 15064	SCR PNPZ ST 18-8 M3 X 16	8.0 EA	
2000 555 00001	CAP 1N 20% 500V CER F/T	2.0 EA	C026:C027
2522 178 13059	SCR PNPZ ST 18-8 M3 X 8	6.0 EA	
2522 600 79017	WSH PLN FRM A ST 18-8 M3	6.0 EA	

Table 3-45. PCB ASSY HARMONIC GENERATOR - 3913 466 78070

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 461 78070	PCB HARMONIC GENERATOR	1.0 EA	010
9335 048 20722	IC CA2820	1.0 EA	A001
2222 123 17229	CAP 22U 40V ELSOL	1.0 EA	
@RD = C001			
2022 552 01178	CAP 5N1 10% 50V 700B	2.0 EA	C002 C019
2222 682 34399	CAP 39P 2% 100V N150 0.1"	1.0 EA	C003
2222 682 34229	CAP 22P 2% 100V N150 0.1"	1.0 EA	C004
2022 554 00283	CAP 22P 10% 500V 100B	1.0 EA	C013
2222 682 34279	CAP 27P 2% 100V N150 0.1"	1.0 EA	C005
2222 629 18103	CAP 10N -20+80 63V HI-K 0.1"	1.0 EA	C006
2000 800 00006	CAP TRIM 25P-500P PCB MGT	2.0 EA	C007 C008
2022 554 00855	CAP 220P 10% 200V 100B	2.0 EA	C009 C010
2022 554 00854	CAP 300P 5% 200V 100B	2.0 EA	C011 C012
2013 017 01543	CAP 10U 20% 16V TANT	1.0 EA	C018
2222 682 10109	CAP 10P 2% 100V NPO 0.1"	1.0 EA	C020
2013 555 01101	CAP 1N0 -20+80 400V F/T	2.0 EA	C021 C022
2022 554 00285	CAP 100P 10 500V 100B	1.0 EA	C027
2413 535 00199	CHOKE 33UH 0W33 BS9751-N0001-C	3.0 EA	0000 L001 L002 L003
3913 469 02050	COIL	1.0 EA	L004
3913 469 01290	COIL	1.0 EA	L005
3913 469 01030	COIL	1.0 EA	L006
2413 535 00419	CHOKE 100UH 0W33 BS9751-N001-D	2.0 EA	L007:L008
2122 102 00148	RES 470R 10% W125 CRBCMP	2.0 EA	R001 R003
2122 102 00913	RES 10R 5% W125 CRBCMP	1.0 EA	R002
2122 102 01005	RES 100R 5% W125 CRBCMP	2.0 EA	R004 R005
2122 102 01007	RES 330R 5% W125 CRBCMP	1.0 EA	R006
2122 102 01185	RES 39R 5% W125 CRBCMP	1.0 EA	
@RD = R007			
2122 102 00584	RES 150R 5% W125 CRBCMP	1.0 EA	R008
2122 102 00597	RES 220R 5% W125 CRBCMP	1.0 EA	R014
2122 362 00141	POT 200R 10% LIN W5	1.0 EA	R009
2322 156 18201	RES 820R 1% 0W6 MTLFLM	1.0 EA	R010
2322 156 13901	RES 390R 1% 0W6 MTLFLM	1.0 EA	R011
9330 000 80112	DIODE OA91	1.0 EA	V001
9338 828 03682	DIODE 5082-0800/MA43000-103	1.0 EA	V002

2413 015 02201	PIN TEST 1.3 X 1.02MM PCB	2.0 PK	TP01:TP02
2422 024 00305	SKT 1 WAY PCB	9.0 EA	350
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	3.0 EA	360
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	2.0 EA	

Table 3-46. CASE ASSY - 3913 467 13230

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 464 19270	PLATE FRONT	1.0 EA	
3913 464 19280	PLATE REAR	1.0 EA	
3913 464 19290	SUPPORT BAR L/H PCB	1.0 EA	
3913 464 19310	COVER	1.0 EA	
3913 464 19300	SUPPORT BAR R/H PCB	1.0 EA	
2522 178 13059	SCR PNPZ ST 18-8 M3 X 8	4.0 EA	045
2522 178 15058	SCR PNPZ ST 18-8 M3 X 6	12.0 EA	
2513 712 02004	WSH CRKL ST 18-8 M3	16.0 EA	

Table 3-47. SOUND MODULATOR - 3913 467 13940

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 467 13950	CASE (SND MOD)	1.0 EA	001
3913 466 78550	PCB ASSY SOUND MODULATOR	1.0 EA	002
2522 163 40005	SCR PNPZ ZN S/T-AB 4X1/4	6.0 EA	
@RD = 003			
2422 034 16776	CONTACT SKT 22-20 AWG	10.0 EA	004 CBL 2 CORE 7/0.1 SCR N 0713 291 01005 A/ REQD CBL 1CORE 7/0.1 SCRN 0713 291 00002 A/ REQD
0722 100 34005	CBL RF 50R RG178B/U TO MIL-C-1	1.50 RL	006
2413 015 01384	TAG SOLDER 2BA	9.0 PK	007
2522 600 79017	WSH PLN FRM A ST 18-8 M3	2.0 EA	008
2432 020 00234	PLUG RF SMB 50R B/H SLDR	9.0 EA	X001 X002 X003 X004 X006 X007 X008 X009 X011
2422 025 02804	SKT 12 WAY (QIKMATE)	1.0 EA	X005
2422 026 03338	PLUG 3 WAY PANEL MTG	1.0 EA	X010
2522 178 15059	SCR PNPZ ST ZN M3 X 8	2.0 EA	120
2522 401 50008	NUT FULL HEX ST 18-8 M3	2.0 EA	130
2513 712 02004	WSH CRKL ST 18-8 M3	2.0 EA	140

Table 3-48. PCB ASSY SOUND MODULATOR - 3913 466 78550

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 461 78550	PCB - TV SOUND MODULATOR	1.0 EA	0010
2413 015 14168	TAG SOLDER PCB TAIL 2.5 X 0.9M	26.0 EA	006
2413 015 14169	TAG SOLDER PCB TAIL 2.5 X 1.3M	27.0 EA	007
3913 445 50120	HEADER 1 X 3	9.0 EA	008
2422 549 26016	SKT 2 WAY 2.54MM PITCH	8.0 EA	009
2412 490 00119	LED MOUNTING	3.0 EA	010
2413 535 02011	CAN SCREENING ALUM	4.0 EA	FOR L1,2,3,4.
9335 327 60682	IC TL072CP (DIL-8)	6.0 EA	A001 A002 A003 A010 A012 A013
9337 986 20682	IC DG212CJ	1.0 EA	A004
9333 242 60602	IC HEF4069UBP	1.0 EA	A005
9335 598 80602	IC HEF4060BP	2.0 EA	A006 A008
9332 966 90602	IC HEF4046BP	1.0 EA	A007
@PN = 9333 243 30602	**IC HEF4528BP**	**1.0 EA**	A009
9335 266 50602	IC NE5532N DIL-8	1.0 EA	A011
9332 912 10602	IC MC1496P	1.0 EA	A014
9336 772 00682	IC SL560CDP (DIL-8)	4.0 EA	A015 A016 A017 A018

9336 056 80682	IC LM317LZ (TO-92)	1.0 EA	A019
9335 950 60682	IC TL071ACP	1.0 EA	A020
9335 825 80682	IC ULN2004A DIL-16	1.0 EA	A021
2013 017 01525	CAP 100U 20% 10V TANT	3.0 EA	C001 C002 C116
2012 310 00318	CAP 100N 10% 63V PSTR 0.2"	48.0 EA	C003 C020 C023 C031 C058 C062 C064 C065 C066 C067 C068 C069 C070 C072 C074 C076 C077 C078 C080 C081 C082 C083 C085 C086 C087 C088 C089 C090 C091 C092 C093 C094 C095 C096 C097 C098 C099 C101 C102 C103 C105 C106 C107 C111 C112 C117 C118 C121
2013 017 01551	CAP 15U 20% 16V TANT	10.0 EA	C004 C006 C007 C060 C071 C073 C075 C084 C114 C122
2013 751 15328	CAP 6N2 1% 100/125V MICA	1.0 EA	C005
2222 630 19472	CAP 4N7 10% 100V MED-K 0.2"	22.0 EA	C008 C022 C027 C028 C029 C030 C039 C040 C041 C042 C043 C044 C045 C046 C048 C049 C050 C051 C079 C108 C110 C115
2222 683 34121	CAP 120P 2% 100V N150 0.2"	5.0 EA	C009 C010 C032 C034 C036
2222 683 34101	CAP 100P 2% 100V N150 0.2"	2.0 EA	C011 C047
2222 683 58221	CAP 220P 2% 100V N750 0.2"	1.0 EA	C012
2222 683 09688	CAP 6P8 0.25PF 100V NPO 0.2"	1.0 EA	C013
2222 683 34569	CAP 56P 2% 100V N150 0.2"	2.0 EA	C014 C052
2222 809 05002	CAP 1P8 - 10P TRIM (10E)	1.0 EA	C015
2012 310 00323	CAP 470N 20% 63V PSTR 0.2" P	4.0 EA	C016 C024 C026 C119
2022 035 00002	CAP 500U 25V ELECT	1.0 EA	C017
@PN = 2222 683 34339	**CAP 33P 2% 100V N150 0.2"**	**3.0 EA**	
			C018 C053 C104
2222 683 58181	CAP 180P 2% 100V N750 0.2"	2.0 EA	C019 C021
2012 310 03162	CAP 1U0 10% 50V PSTR 0.2" P	2.0 EA	C025 C059
2013 751 15582	CAP 1N0 1% 350/400V MICA	1.0 EA	C054
2222 683 34829	CAP 82P 2% 100V N150 0.2"	3.0 EA	C055 C056 C057
2222 031 35471	CAP 470U 16V ELECT	2.0 EA	C061 C063
2222 630 19561	CAP 560P 10% 100V MED-K 0.2"	1.0 EA	C100
2222 683 09478	CAP 4P7 0.25PF 100V NPO 0.2"	1.0 EA	C109
2222 683 10189	CAP 18P 2% 100V NPO 0.2"	1.0 EA	C120
9332 897 10682	LED 5MM HLMP-3507 GRN	1.0 EA	H001
9332 897 20682	LED 5MM HLMP-3301 RED	2.0 EA	H002 H003
3913 074 51020	CRYSTAL 4.5000MHZ	1.0 EA	B001
3913 469 50140	CHOKE RF (6 HOLE FORMER)	2.0 EA	L009 L010
2413 535 00421	CHOKE 470UH 0W33 BS9751-N001-D	6.0 EA	L011 L013 L014 L015 L016 L018
3913 469 02740	COIL 12 TURNS(ON TORROID)	2.0 EA	L012 L017
2322 156 15602	RES 5K6 1% 0W6 MTLFLM	2.0 EA	R001 R138
2322 156 13609	RES 36R 1% 0W6 MTLFLM	2.0 EA	R002 R003
2322 156 16201	RES 620R 1% 0W6 MTLFLM	5.0 EA	R004 R084 R085 R150 R157
2322 156 11003	RES 10K 1% 0W6 MTLFLM	37.0 EA	R005 R015 R022 R044 R045 R046 R053 R056 R060 R062 R071 R074 R077 R081 R086 R091 R098 R112 R114 R116 R117 R118 R119 R123 R126 R127 R129 R130 R131 R142 R143 R144 R145 R146 R155 R049 R136
2322 156 16802	RES 6K8 1% 0W6 MTLFLM	1.0 EA	R006
2322 156 13302	RES 3K3 1% 0W6 MTLFLM	2.0 EA	
@RD = R007 R029			
2322 156 14702	RES 4K7 1% 0W6 MTLFLM	9.0 EA	R008 R039 R061 R087 R106 R125 R148 R159 R018
2122 350 00354	POT 1K0 20% LIN W5	1.0 EA	R009

2122 350 00372	POT 5K0 10% LIN W5 SIDE ADJ	1.0 EA	R010
2322 156 12204	RES 220K 1% 0W6 MTLFLM	2.0 EA	R011 R147
2322 156 14703	RES 47K 1% 0W6 MTLFLM	3.0 EA	R013 R102 R156
2322 156 18201	RES 820R 1% 0W6 MTLFLM	2.0 EA	R014 R068
2122 350 00459	POT 10K 10% LIN W5 SIDE ADJ	3.0 EA	R016 R017 R165
2322 156 12202	RES 2K2 1% 0W6 MTLFLM	8.0 EA	R021 R034 R052 R058 R064 R089 R097 R124
2322 156 11002	RES 1K 1% 0W6 MTLFLM	8.0 EA	R023 R026 R040 R050 R054 R069 R141 R158
2322 156 11502	RES 1K5 1% 0W6 MTLFLM	1.0 EA	R024
2322 156 12201	RES 220R 1% 0W6 MTLFLM	6.0 EA	R025 R027 R083 R093 R099 R109
2322 156 14701	RES 470R 1% 0W6 MTLFLM	4.0 EA	R028 R035 R057 R090
2322 156 12203	RES 22K 1% 0W6 MTLFLM	5.0 EA	R030 R031 R132 R019 R166
2322 156 17501	RES 750R 1% 0W6 MTLFLM	5.0 EA	R032 R063 R120 R121 R122
2322 156 13304	RES 330K 1% 0W6 MTLFLM	2.0 EA	R033 R042
2322 241 13106	RES 10M 5% 0W25 MTLGLZ	1.0 EA	R036
2322 156 11004	RES 100K 1% 0W6 MTLFLM	7.0 EA	R037 R038 R100 R101 R111 R128 R137
2322 156 16801	RES 680R 1% 0W6 MTLFLM	2.0 EA	0000 R041 R080
2322 241 13105	RES 1M 5% 0W25 MTLGLZ	2.0 EA	0000 R047 R115
2322 156 12702	RES 2K7 1% 0W6 MTLFLM	1.0 EA	R051
2322 156 11001	RES 100R 1% 0W6 MTLFLM	11.0 EA	R055 R070 R073 R094 R095 R096 R103 R105 R107 R140 R152
2122 350 00361	POT 10K 20% LIN W5	1.0 EA	R059
2322 156 17509	RES 75R 1% 0W6 MTLFLM	8.0 EA	R065 R067 R088 R153 R154 R162 R163 R164
2322 156 11201	RES 120R 1% 0W6 MTLFLM	1.0 EA	R066
2122 362 00148	POT 50K 10% LIN W5 TOP ADJ	1.0 EA	R072
@PN = 2322 156 15109	**RES 51R 1% 0W6 MTLFLM**	**2.0 EA**	R075 R151
2322 156 11302	RES 1K3 1% 0W6 MTLFLM	1.0 EA	R076
2322 156 13002	RES 3K 1% 0W6 MTLFLM	2.0 EA	R078 R079
2322 156 12208	RES 2R2 1% 0W6 MTLFLM	1.0 EA	R082
2322 156 11501	RES 150R 1% 0W6 MTLFLM	1.0 EA	R092
2122 350 00363	POT 5K0 20% LIN W5	3.0 EA	R104 R133 R139
2122 350 00414	POT 500R 10% LIN W5 SIDE ADJ	1.0 EA	R108
2322 156 14709	RES 47R 1% 0W6 MTLFLM	1.0 EA	R110
2322 156 11504	RES 150K 1% 0W6 MTLFLM	1.0 EA	R113:
2322 156 11803	RES 18K 1% 0W6 MTLFLM	2.0 EA	R020 R134
2322 156 11503	RES 15K 1% 0W6 MTLFLM	3.0 EA	R012 R048 R135
2322 156 11005	RES 1M 1% 0W6 MTLFLM	1.0 EA	R160
9334 013 30682	TRANS J310	1.0 EA	V001
9334 607 30112	DIODE BB212	1.0 EA	V002
9334 357 00765	DIODE 5082-3379	3.0 EA	V003 V009 V014
9330 765 30112	TRANS BFX89	6.0 EA	V004 V005 V006 V007 V024 V031
9330 473 10112	DIODE 1N916	13.0 EA	V008 V015 V016 V017 V018 V019 V021 V022 V025 V026 V028 V030 V032
9332 014 30682	DIODE 5082-2805 (MATCHED QUA	1.0 EA	V010 V011 V012 V013
9331 177 30112	DIODE BZX79C5V6	1.0 EA	V020
9331 177 20112	DIODE BZX79C5V1	1.0 EA	V023
9330 093 20112	DIODE BZY88C8V2	1.0 EA	V027
9334 989 80702	TRANS MPSA06	1.0 EA	V029
2222 683 09278	CAP 2P7 0.25PF 100V NPO 0.2"	3.0 EA	C033 C035 C037
2222 683 10101	CAP 100P 2% 100V NPO 0.2"	1.0 EA	C038
3913 469 50340	COIL 4.80-10.5UH	2.0 EA	L002 L004
@PN = 3913 469 50870	**COIL 44.6-48.5UH**	**1.0 EA**	L003
3913 469 04090	COIL 3 TURNS	4.0 EA	L005 L006 L007 L008

WARNING:Disconnect primary power prior to servicing

3913 469 51010	COIL 3.2-6.7UH	1.0 EA	L001
2322 156 17503	RES 75K 1% 0W6 MTLFLM	1.0 EA	R149
2322 156 13303	RES 33K 1% 0W6 MTLFLM	1.0 EA	R043

Table 3-49. CASE (SND MOD) - 3913 467 13950

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
3913 465 53400	EXTRUSION - TOP	1.0 EA	001
3913 465 53390	EXTRUSION(BOTTOM)	1.0 EA	002
3913 464 20180	LABEL STRIP - (IC SOUND MODULA	1.0 EA	003
3913 464 19000	PLATE	1.0 EA	
3913 464 09110	COVER SIDE	1.0 EA	004
3913 464 08930	PANEL - FRONT	1.0 EA	005
3913 464 09000	PANEL - REAR	1.0 EA	006
3913 464 09030	COVER SIDE (BLANK)	1.0 EA	007
2500 708 98002	NUT No:4 ANGLE “SPIRE”	4.0 EA	009
3913 464 05120	CLIP RETAINING	2.0 EA	010
3913 463 20860	COVER	1.0 EA	011
3913 463 20780	MNTG BRKT	1.0 EA	012
2522 187 02046	SCR CSKSL ST ZN M2.5X10	8.0 EA	016
302 0632 000	SCR CSK PHIL 10-32 X 5/8 SST	1.0 EA	
2522 178 15038	SCR PNPZ ST 18-8 M2 X 6	1.0 EA	018
2522 163 01005	SCR PNPZ ZN S/T-B 4X1/4	7.0 EA	020
2513 712 02007	WSH CRKL ST 18-8 M6	1.0 EA	022
2513 712 02004	WSH CRKL ST 18-8 M3	6.0 EA	023
357 0104 000	SPACER, 10-32 X 0.625 LG	1.0 PC	
2522 401 50008	NUT FULL HEX ST 18-8 M3	2.0 EA	026
2522 177 04019	SCR PNSL ST ZN M2X6	4.0 EA	
@RD = 029			
2512 795 02005	WSH SCHNR STNI M2.3	4.0 EA	030
2522 401 60005	NUT FULL HEX ST 18-8 M2	4.0 EA	031
2522 401 60064	NUT FULL HEX ST 18-8 M2	1.0 EA	251
2513 712 02003	WSH CRKL ST 18-8 M2.5	1.0 EA	260

Table 3-50. PCB-RF DIST AMP 3 WAY - 3913 466 78060

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
9338 827 24682	OBS, IC OM2070	3.0 EA	A001 A002 A003
9340 000 70682	DIODE DAA5126-400-001	1.0 EA	A006
2000 501 03331	CAP 330P 5% 50V NPO CER 1206	18.0 EA	C012 C001 C002 C004 C006 C007 C008 C009 C010 C011 C013 C014 C018 C022 C023 C024 C025 C027
2000 501 11104	CAP 100N 10% 50V X7R CER 1206	1.0 EA	C003
2000 501 01478	CAP 4P7 0P5 50V NPO CER 1206	1.0 EA	C026
2000 075 04109	CAP 10U 10% 16V TANT Size C	1.0 EA	C005
2400 535 10014	INDUCTOR 0.1uH 10% SIZE 1210	7.0 EA	L001 L002 L003 L004 L005 L007 L009
2100 700 05331	RES 330R 5% 0.25W Size 1206	2.0 EA	R001 R003
2100 700 05159	RES 15R 5% 0.25W Size 1206	2.0 EA	R002 R032
2100 700 05241	RES 240R 5% 0.25W Size 1206	3.0 EA	R004 R005 R029
2100 700 05301	RES 300R 5% 0.25W Size 1206	1.0 EA	R006
2100 700 99999	RES 0R Jumper Size 1206	3.0 EA	NOMINAL VALUE R13:R16:R19:
2100 700 05181	RES 180R 5% 0.25W Size 1206	1.0 EA	R033
2100 700 05478	RES 4R7 5% 0.25W Size 1206	1.0 EA	R034
2100 700 05202	RES 2K 5% 0.25W Size 1206	1.0 EA	
@RD = R030			
2100 700 05222	RES 2K2 5% 0.25W Size 1206	1.0 EA	R031
2100 700 05101	RES 100R 5% 0.25W Size 1206	4.0 EA	R007:R008:R009:R011
2122 362 00159	POT 10K 10% LIN W5 TOP ADJ	1.0 EA	R012

9340 000 40682	DIODE BZX84-C4V7 (MARK-Z1	1.0 EA	V001
9340 000 10682	TRANS BC847B (MARK-1F)	1.0 EA	V002
9340 000 00682	TRANS BFG197 (MARK-V5	1.0 EA	V003
2400 031 00011	SKT RF SMC 50R PCB MTG STRGHT	4.0 EA	X001 X002 X003 X004
2422 025 02884	HEADER 3 WAY 0.1" PITCH	1.0 EA	X007
3913 461 78060	PCB-RF DIST AMP 2-5 WAY	1.0 EA	
922 1206 091	LID PCB-RF DIST AMP	1.0 EA	
922 1206 090	SHIELD STRIP PCB-RF DIST AMP	1.0 EA	

Table 3-51. RF DIST AMP PCB 4WAY (ULTRA) - 3913 467 14650

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
9338 827 24682	OBS, IC OM2070	4.0 EA	A001:A002:A003:A004
9340 000 70682	DIODE DAA5126-400-001	1.0 EA	A006
2000 501 03331	CAP 330P 5% 50V NPO CER 1206	21.0 EA	C001:C002:C004:C006:C007:C008:C009: C010:C011:C012:C013:C0 14:C015:C016: C017:C018: C022:C023:C024:C025: C027
2000 501 11104	CAP 100N 10% 50V X7R CER 1206	1.0 EA	C003
2000 501 01478	CAP 4P7 0P5 50V NPO CER 1206	1.0 EA	C026
2000 075 04109	CAP 10U 10% 16V TANT Size C	1.0 EA	C005
2400 535 10014	INDUCTOR 0.1uH 10% SIZE 1210	8.0 EA	L001:L002:L003:L004:L005:L006:L007: L009
2100 700 05331	RES 330R 5% 0.25W Size 1206	2.0 EA	R001 R003
@PN = 2100 700 05159	**RES 15R 5% 0.25W Size 1206**	**2.0 EA**	R002 R032
2100 700 05241	RES 240R 5% 0.25W Size 1206	3.0 EA	R004 R005 R029
2100 700 05301	RES 300R 5% 0.25W Size 1206	1.0 EA	R006
2100 700 99999	RES 0R Jumper Size 1206	2.0 EA	NOMINAL VALUE R019:R022
2100 700 05181	RES 180R 5% 0.25W Size 1206	1.0 EA	R033
2100 700 05478	RES 4R7 5% 0.25W Size 1206	1.0 EA	R034
2100 700 05202	RES 2K 5% 0.25W Size 1206	1.0 EA	R030
2100 700 05222	RES 2K2 5% 0.25W Size 1206	1.0 EA	R031
2100 700 05101	RES 100R 5% 0.25W Size 1206	1.0 EA	R011
2100 700 05151	RES 150R 5% 0.25W Size 1206	4.0 EA	R007:R008:R009:R010
2100 700 05271	RES 270R 5% 0.25W Size 1206	4.0 EA	R014:R015:R017:R018
2100 700 05189	RES 18R 5% 0.25W Size 1206	2.0 EA	R013:R016
2122 362 00159	POT 10K 10% LIN W5 TOP ADJ	1.0 EA	R012
9340 000 40682	DIODE BZX84-C4V7 (MARK-Z1	1.0 EA	V001
9340 000 10682	TRANS BC847B (MARK-1F)	1.0 EA	V002
9340 000 00682	TRANS BFG197 (MARK-V5	1.0 EA	V003
2400 031 00011	SKT RF SMC 50R PCB MTG STRGHT	5.0 EA	X001:X002:X003:X004: X005
2422 025 02884	HEADER 3 WAY 0.1" PITCH	1.0 EA	X007
3913 461 78060	PCB-RF DIST AMP 2-5 WAY	1.0 EA	
922 1206 091	LID PCB-RF DIST AMP	1.0 EA	
922 1206 090	SHIELD STRIP PCB-RF DIST AMP	1.0 EA	
@RD =			

Table 3-52. C/F IOT EXCITER - 952 9190 286

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
2400 015 00091	TERM BLOCK 6 WAY 4-WIRE	3.0 EA	X018 X019 X020
2400 016 00009	JUMPER BAR-COMB TYPE	12.0 EA	
2422 025 03827	SKT 24 WAY (QIKMATE)	1.0 EA	X008
2422 025 02804	SKT 12 WAY (QIKMATE)	1.0 EA	X009
2422 025 04439	PLUG 12 WAY (QIKMATE)	6.0 EA	AX05:CX05:DX05:EX05: FX05:GX05
2422 034 16118	HOOD 12 WAY (QIKMATE)	6.0 EA	
2422 015 12167	TERM INSULUG M4 RED	7.0 EA	
2422 034 16777	CONTACT PLUG 22-20 AWG	31.0 EA	

2422 034 16776	CONTACT SKT 22-20 AWG	10.0 EA	
2413 016 00322	FERRL B LACE 0.5MM2	45.0 EA	
2422 026 03337	SKT 3 WAY CABLE MTG	1.0 EA	FX10
0724 300 00001	CBL 2 X 7/0.2 PVC SCRN	1.0 RL	
2422 025 01894	HOUSING 3 WAY 0.1" Pitch	2.0 EA	JX07 MX07
2422 034 11905	CONTACT CRIMP (MOLEX) GOLD PLA	8.0 EA	0080
2422 025 02773	HOUSING 6 WAY 0.1" Pitch	1.0 EA	SX09
2413 016 00323	FERRL B LACE 1.0MM2	6.0 EA	0090
0813 026 04136	SLVE PVC 6MM I/D BLK	3.60 ME	0095
2422 034 16778	CONTACT SKT 18-16 AWG	9.0 EA	0100
414 0300 000	FERRITE RING 7mm ID 3C85	9.0 EA	110
0713 291 00001	CBL 1 X 16/0.2 PVC BRAID SCRN	4.50 RL	120

Table 3-53. KIT OF COAX CABLES - 952 9190 287

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
2432 020 00181	PLUG RF SMB 50R CBL CRMP RG316	29.0 EA	AX01:AX02:AX03:AX04:BX01:BX04:CX01: CX02:CX03:CX04:DX01:DX04: EX01:EX02:EX06:EX07:EX09:DX01:DX02: DX04:FX01:FX04:FX08:FX09: GX01:GX04:KX01:KX02: TEST1:TEST2:
2400 031 00014	PLUG RF SMC 50R CBL R/A RG188	9.0 EA	SX02 SX03 SX04 MX01 MX02 MX03 JX01 JX02 JX03
8213 268 79053	PLUG RF TNC FREE 50R	9.0 EA	LX01 LX02 PX01 RX01 RX02 NX01 HX01 NX02 HX02
2432 020 00271	SKT RF BNC B/HD CRMP RG188	17.0 EA	X002:X004:X005:X006:X007:X010:X011: X012:X013:X014:X021:X0 22:X023:X024: X025:TEST1 TEST2:
0722 100 33006	CBL RF 50R RD316	15.0 RL	
0722 102 48006	CBL RF 75R RG179B/U TO MIL-C-1	4.20 RL	
8213 268 79022	PLUG RF BNC CBL CRMP 50R RG223	6.0 EA	X012:X013:X014:X021: X022:X023
0722 100 22001	CBL RF 50R RG223/U TO MIL-C-17	0.550 RL	
2411 027 07529	PLUG RF SMB 50R ELBW CRMP	1.0 EA	FX11

Table 3-54. CHASSIS EXCITER - 939 8121 582

HARRIS P/N	*DESCRIPTION*	*QTY/UM*	*REF. SYMBOLS/EXPLANATIONS*
943 5396 425	CHASSIS DRIVE	1.0 EA	0010
922 1206 215	FRNT LOCATING BAR	1.0 EA	0020
943 5396 424	HINGE	1.0 EA	0040
939 8121 579	REAR SUPPORT	1.0 EA	0050
943 5396 431	FRONT PANEL DRIVE	1.0 EA	0060
2500 622 00004	RIV BRIV 3.2 X 6.41MM ALUM	8.0 EA	0140
303 0164 000	SCREW, SKT BUTTON HD M4X8 S/ST	10.0 EA	
2522 178 15106	SCR PNPZ ST 18-8 M5X12	2.0 EA	
2513 712 02006	WSH CRKL ST 18-8 M5	2.0 EA	
2522 401 50011	NUT FULL HEX ST 18-8 M4	3.0 EA	
2513 712 02005	WSH CRKL ST 18-8 M4	3.0 EA	
943 5396 423	LID	1.0 EA	
@PN = 943 5396 422	**SCREENING BOX**	**1.0 EA**	
943 5396 426	COVER	1.0 EA	
2800 040 00003	SLIDE 605MM OPEN (PAIR)	1.0 EA	
448 1065 000	GRAB HANDLE	2.0 EA	
3913 080 54310	SPCR HEX TP M/F M3X30 BR	5.0 EA	
0300 062 00002	FINGER CNCT STRP 8.6x1.6mm S/A	1.50 EA	

TECHNICAL MANUAL

Exciter System M

8928 117 31310/31320

SigmaPlus™ Transmitter Series

DRAWINGS - 839 8139 198

(Part of 988-8603-001)

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